

VCU128 Evaluation Board

HW-U1-VCU128

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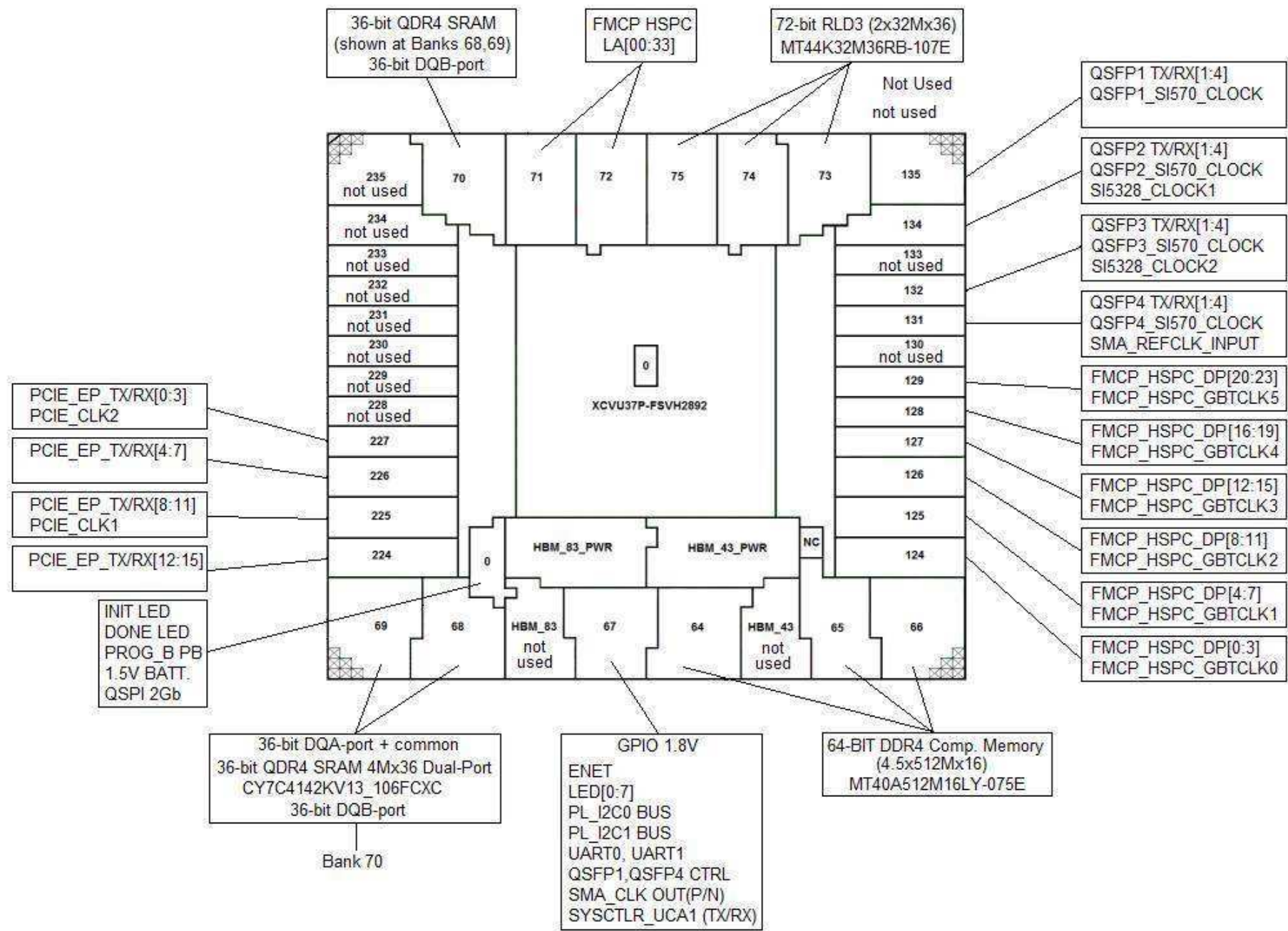
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2100 All Programmable Drive San Jose, CA 95124		ASSY P/N : 0432120	
		TEST P/N : TSS0201	
Title: HW-U1-VCU128			
001 Title Page			Ver 1.0
Size B	Date Modified: Wednesday, October 10, 2018	Document Number: 0381852	Rev 01
Engineer: RO		Sheet 1 of 69	

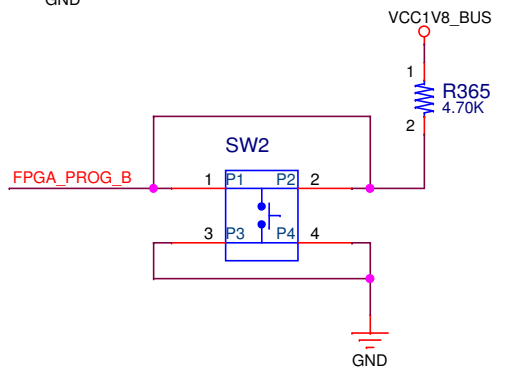
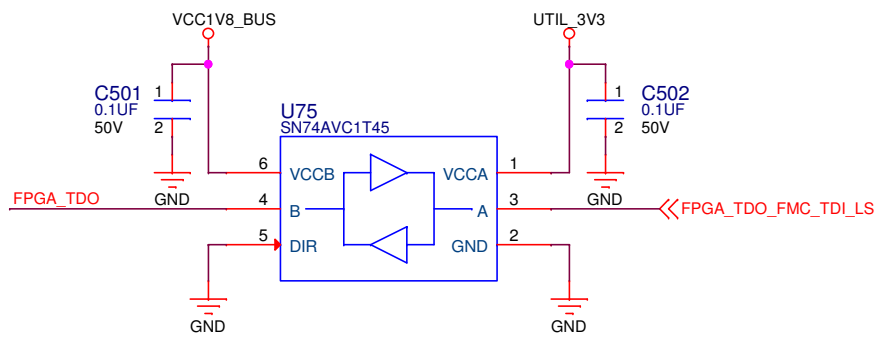
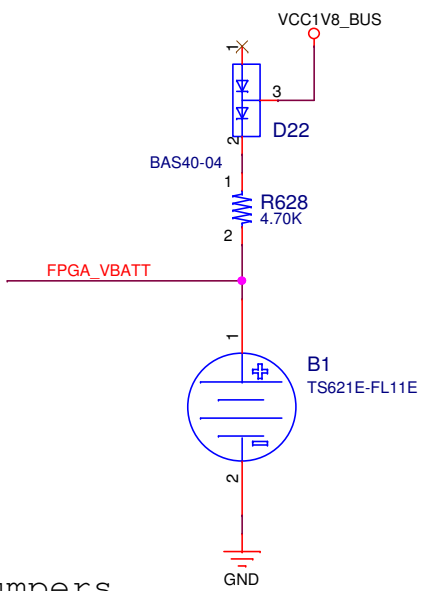
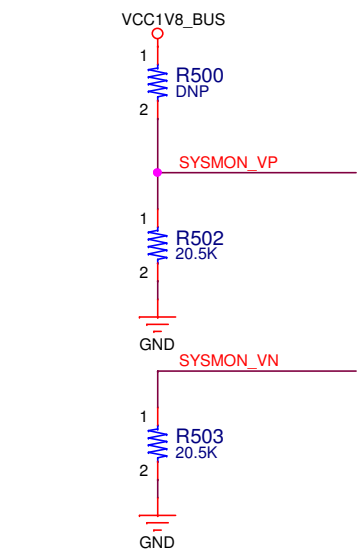
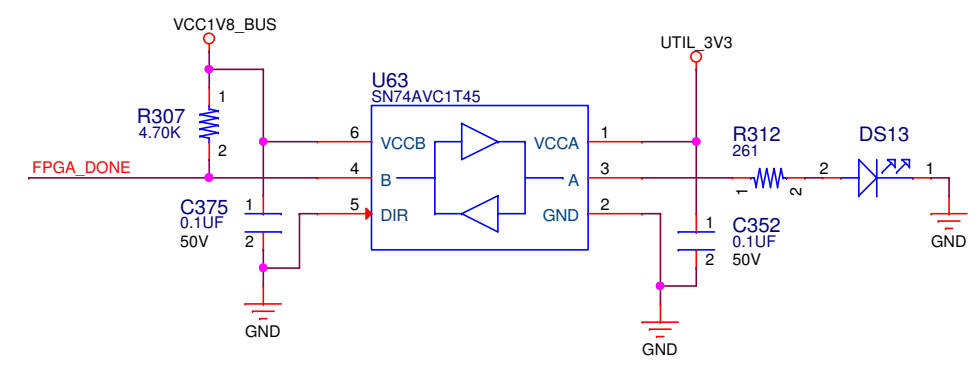
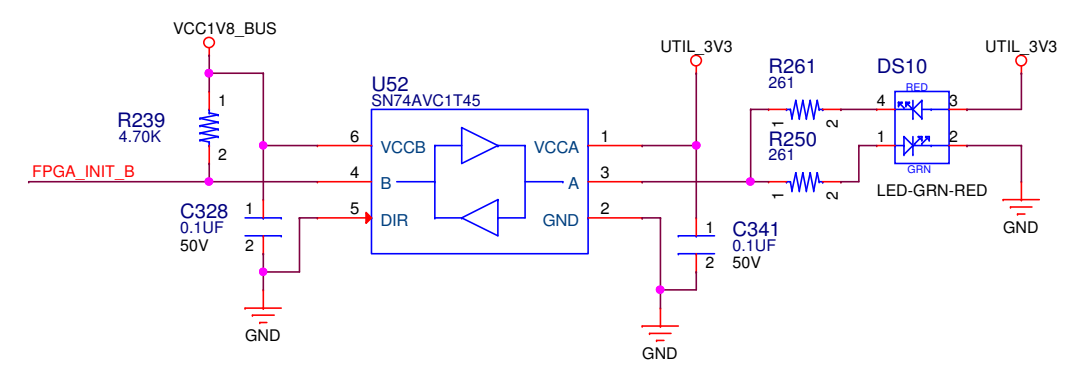
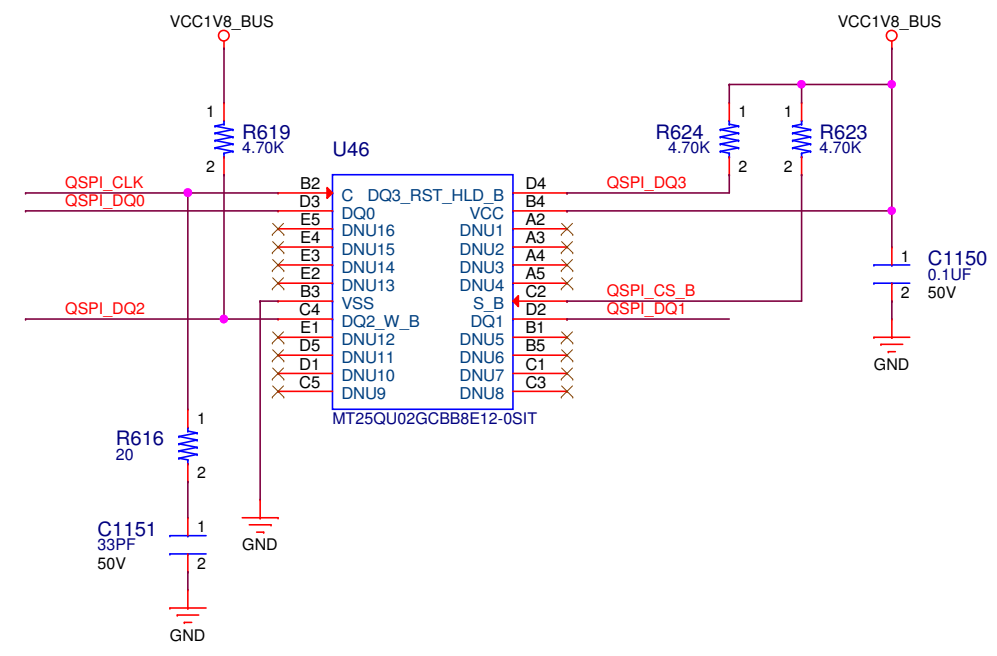
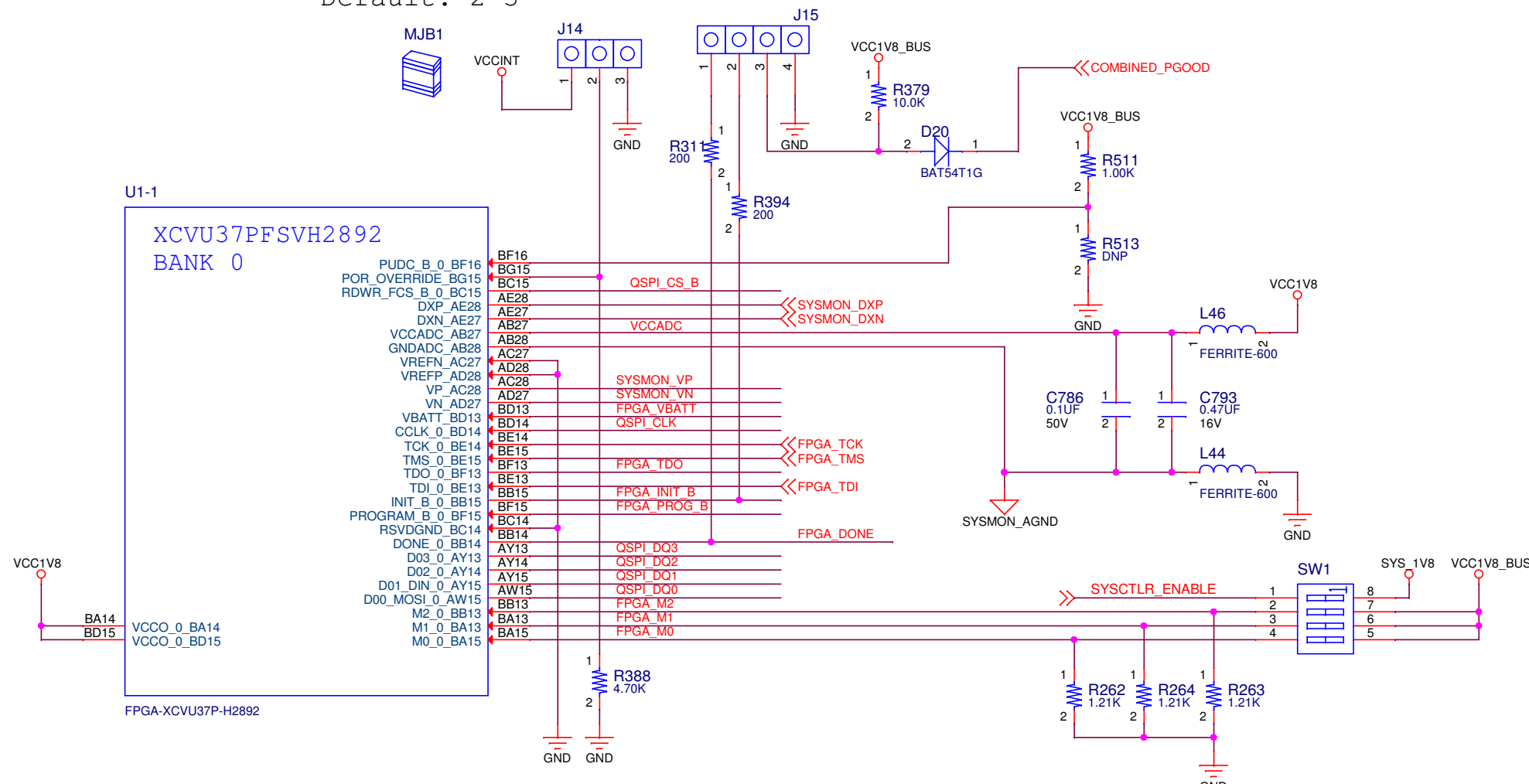


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Title: HW-U1-VCU128 002 Block Diagram		Ver 1.0	
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Default: 2-3

PCIe Test Header



SYSMON I2C Address jumpers

		PCB P/N : 1281016	
2100 All Programmable Drive		ASSY P/N : 0432120	
San Jose, CA 95124		TEST P/N : TSS0201	
Title: HW-U1-VCU128			
003 FPGA Bank 0			
Size B	Date Modified: Wednesday, October 10, 2018	Document Number: 0381852	Ver 1.0
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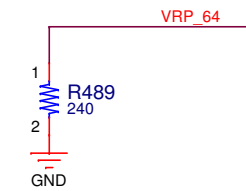
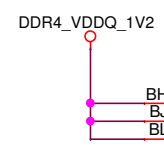
U1-27

XCVU37PFSVH2892
BANK 64

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IO_L24P_T3U_N10_64_BH31
IO_L23N_T3U_N9_64_BF33
IO_L23P_T3U_N8_64_BF32
IO_L22N_T3U_N7_DBC_AD0N_64_BK30
IO_L22P_T3U_N6_DBC_AD0P_64_BJ29
IO_L21N_T3L_N5_AD8N_64_BG32
IO_L21P_T3L_N4_AD8P_64_BF31
IO_L20N_T3L_N3_AD1N_64_BH30
IO_L20P_T3L_N2_AD1P_64_BH29
IO_L19N_T3L_N1_DBC_AD9N_64_BG30
IO_L19P_T3L_N0_DBC_AD9P_64_BG29
IO_T2U_N12_64_BG33
IO_L18N_T2U_N11_AD2N_64_BH35
IO_L18P_T2U_N10_AD2P_64_BH34
IO_L17N_T2U_N9_AD10N_64_BF36
IO_L17P_T2U_N8_AD10P_64_BF35
IO_L16N_T2U_N7_QBC_AD3N_64_BK35
IO_L16P_T2U_N6_QBC_AD3P_64_BK34
IO_L15N_T2L_N5_AD11N_64_BG35
IO_L15P_T2L_N4_AD11P_64_BG34
IO_L14N_T2L_N3_GC_64_BJ34
IO_L14P_T2L_N2_GC_64_BJ33
IO_L13N_T2L_N1_GC_QBC_64_BJ32
IO_L13P_T2L_N0_GC_QBC_64_BH32
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IO_L12N_T1U_N11_GC_64_BL33
IO_L12P_T1U_N10_GC_64_BK33
IO_L11N_T1U_N9_GC_64_BL31
IO_L11P_T1U_N8_GC_64_BK31
IO_L10N_T1U_N7_QBC_AD4N_64_BM35
IO_L10P_T1U_N6_QBC_AD4P_64_BL35
IO_L9N_T1L_N5_AD12N_64_BM33
IO_L9P_T1L_N4_AD12P_64_BL32
IO_L8N_T1L_N3_AD5N_64_BP34
IO_L8P_T1L_N2_AD5P_64_BN34
IO_L7N_T1L_N1_QBC_AD13N_64_BN35
IO_L7P_T1L_N0_QBC_AD13P_64_BM34
IO_T0U_N12_VRP_64_BM32
IO_L6N_T0U_N11_AD6N_64_BP32
IO_L6P_T0U_N10_AD6P_64_BN32
IO_L5N_T0U_N9_AD14N_64_BM30
IO_L5P_T0U_N8_AD14P_64_BL30
IO_L4N_T0U_N7_DBC_AD7N_64_BN30
IO_L4P_T0U_N6_DBC_AD7P_64_BN29
IO_L3N_T0L_N5_AD15N_64_BP31
IO_L3P_T0L_N4_AD15P_64_BN31
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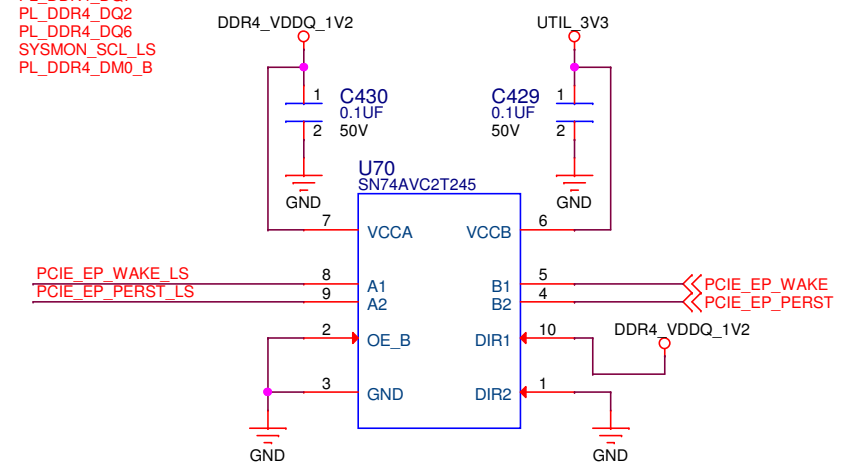
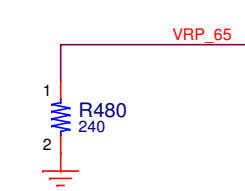
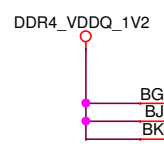
U1-28

XCVU37PFSVH2892
BANK 65

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IO_L23P_T3U_N8_I2C_SCLK_65_BC42
IO_L22N_T3U_N7_DBC_AD0N_D05_65_BE46
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IO_L21N_T3L_N5_AD8N_D07_65_BF43
IO_L21P_T3L_N4_AD8P_D06_65_BF42
IO_L20N_T3L_N3_AD1N_D09_65_BF46
IO_L20P_T3L_N2_AD1P_D08_65_BF45
IO_L19N_T3L_N1_DBC_AD9N_D11_65_BE41
IO_L19P_T3L_N0_DBC_AD9P_D10_65_BD41
IO_T2U_N12_CSI_ADV_B_65_BH41
IO_L18N_T2U_N11_AD2N_D13_65_BG45
IO_L18P_T2U_N10_AD2P_D12_65_BG44
IO_L17N_T2U_N9_AD10N_D15_65_BG43
IO_L17P_T2U_N8_AD10P_D14_65_BG42
IO_L16N_T2U_N7_QBC_AD3N_A01_D17_65_BJ46
IO_L16P_T2U_N6_QBC_AD3P_A00_D16_65_BH46
IO_L15N_T2L_N5_AD11N_A03_D19_65_BK41
IO_L15P_T2L_N4_AD11P_A02_D18_65_BJ41
IO_L14N_T2L_N3_GC_A05_D21_65_BH45
IO_L14P_T2L_N2_GC_A04_D20_65_BH44
IO_L13N_T2L_N1_GC_QBC_A07_D23_65_BJ42
IO_L13P_T2L_N0_GC_QBC_A06_D22_65_BH42
IO_T1U_N12_SMBALERT_65_BM42
IO_L12N_T1U_N11_GC_A09_D25_65_BJ44
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IO_L9N_T1L_N5_AD12N_A15_D31_65_BL43
IO_L9P_T1L_N4_AD12P_A14_D30_65_BL42
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IO_L8P_T1L_N2_AD5P_A16_65_BL45
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IO_L7P_T1L_N0_QBC_AD13P_A18_65_BL47
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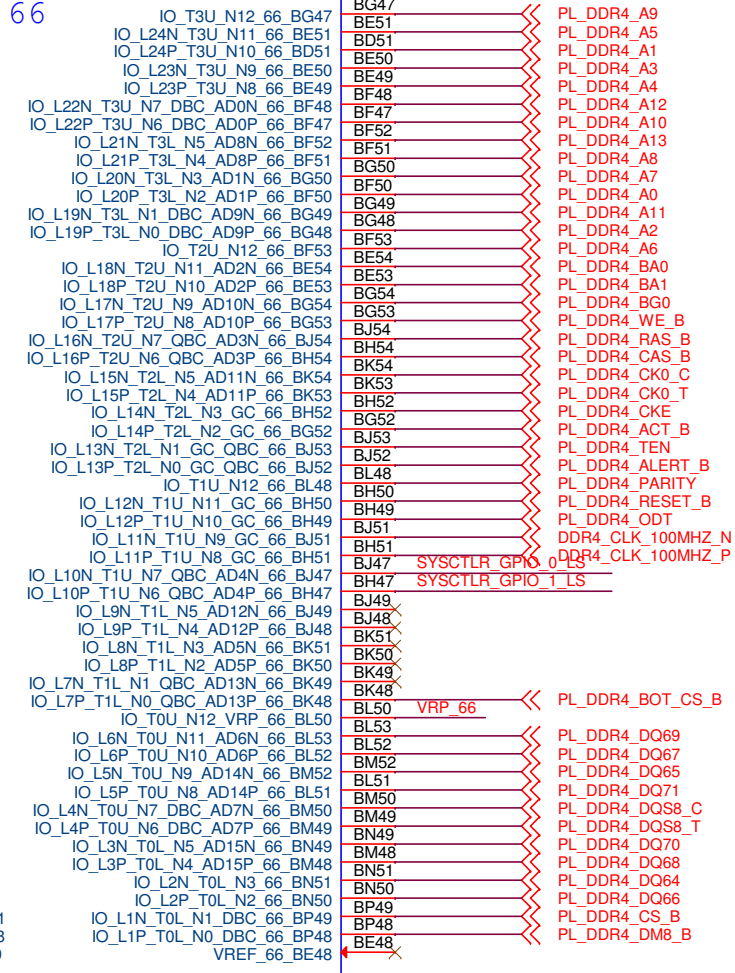
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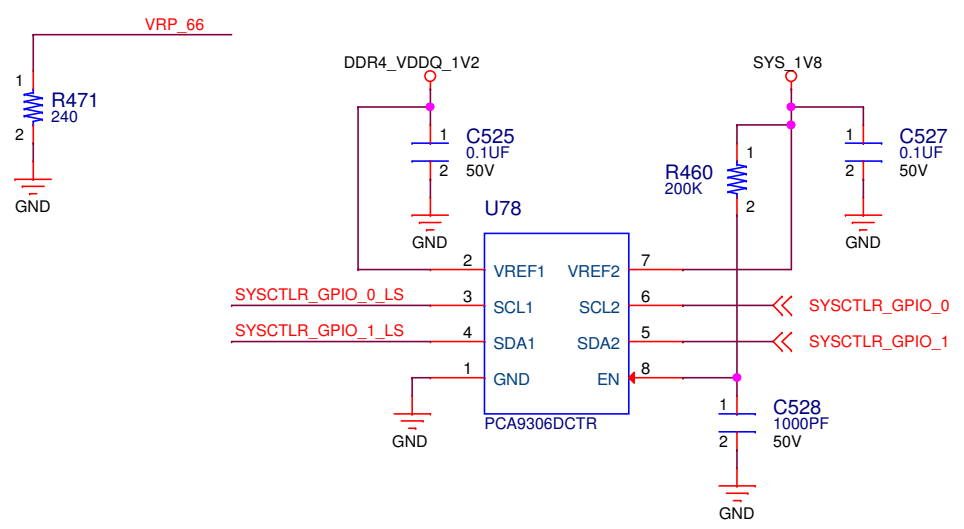
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BANK 66

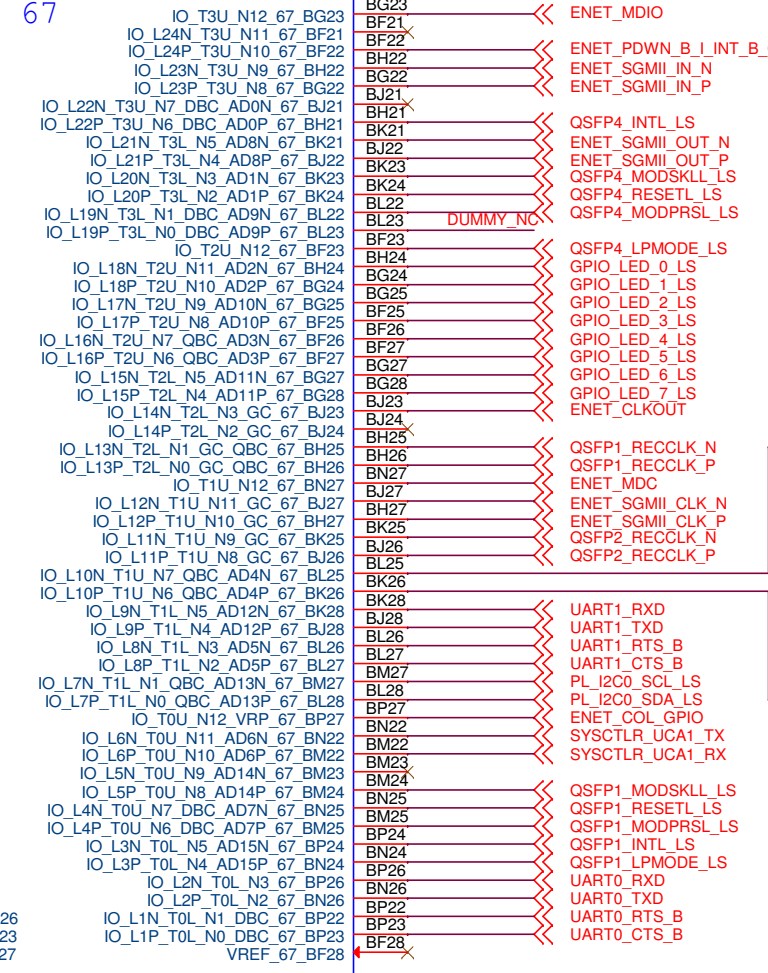


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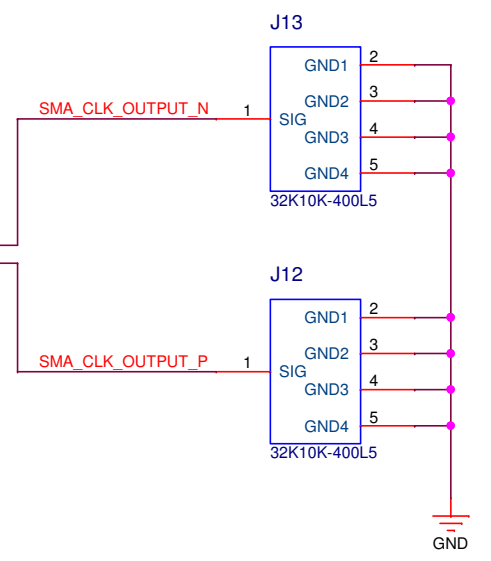
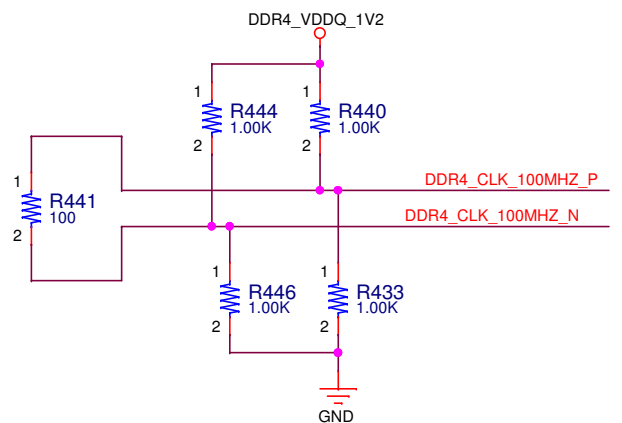


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XCVU37PFSVH2892
BANK 67



FPGA-XCVU37P-H2892



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Title: HW-U1-VCU128 005 FPGA Bank 66 67			
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XCVU37PFSVH2892
BANK 68

IO_T3U_N12_68_BH11
IO_L24N_T3U_N11_68_BE9
IO_L24P_T3U_N10_68_BE10
IO_L23N_T3U_N9_68_BF10
IO_L23P_T3U_N8_68_BE11
IO_L22N_T3U_N7_DBC_AD0N_68_BF11
IO_L22P_T3U_N6_DBC_AD0P_68_BF12
IO_L21N_T3L_N5_AD8N_68_BG9
IO_L21P_T3L_N4_AD8P_68_BG10
IO_L20N_T3L_N3_AD1N_68_BG12
IO_L20P_T3L_N2_AD1P_68_BG13
IO_L19N_T3L_N1_DBC_AD9N_68_BH9
IO_L19P_T3L_N0_DBC_AD9P_68_BH10
IO_T2U_N12_68_BH12
IO_L18N_T2U_N11_AD2N_68_BH14
IO_L18P_T2U_N10_AD2P_68_BH15
IO_L17N_T2U_N9_AD10N_68_BJ12
IO_L17P_T2U_N8_AD10P_68_BJ13
IO_L16N_T2U_N7_QBC_AD3N_68_BK13
IO_L16P_T2U_N6_QBC_AD3P_68_BJ14
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IO_L1N_T0L_N1_DBC_68_BP11
IO_L1P_T0L_N0_DBC_68_BP12
VREF_68_BG14

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BE10 QDR4_DQA28
BF10 QDR4_DQA31
BE11 QDR4_DQA30
BF11 SI5328_INT_ALM_LS
BF12 QDR4_DQA35
BG9 QDR4_DQA33
BG10 QDR4_DQA34
BG12 QDR4_DQA32
BG13 QDR4_DQA29
BH9 QDR4_DKA1_N
BH10 QDR4_DKA1_P
BH12
BH14 QDR4_DQA23
BH15 QDR4_DQA24
BJ12 QDR4_DQA20
BJ13 QDR4_DQA26
BK13 QDR4_QVDA1
BJ14 QDR4_DQA25
BK14 QDR4_DQA19
BK15 QDR4_DQA21
BL12 QDR4_DQA18
BL13 QDR4_DQA17
BK11 QDR4_QKA1_N
BJ11 QDR4_QKA1_P
BL11
BK9
BJ9 QDR4_DQA10
BL10 QDR4_DQA17
BK10 QDR4_DQA11
BM8 QDR4_DQA12
BL8 QDR4_QVDA0
BN9 QDR4_DQA13
BM9 QDR4_DQA16
BN10 QDR4_DQA9
BM10 QDR4_DQA14
BP8 QDR4_DQA15
BP9 QDR4_QKA0_N
BN11 VRP_68 QDR4_QKA0_P
BM15 QDR4_DQA4
BL15 QDR4_DQA8
BM13 QDR4_DQA1
BM14 QDR4_DQA0
BN14 SI5328_RST_B_LS
BN15 QDR4_DQA2
BN12 QDR4_DQA3
BM12 QDR4_DQA7
BP13 QDR4_DQA5
BP14 QDR4_DQA6
BP11 QDR4_DKA0_N
BP12 QDR4_DKA0_P
BG14

QDR4_VDDQ_1V2
BH13
BJ10
BL14
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VCCO_68_BJ10
VCCO_68_BL14

FPGA-XCVU37P-H2892

U1-32

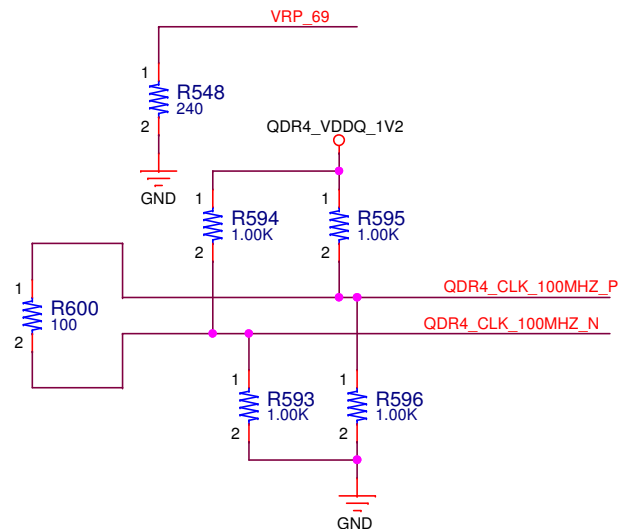
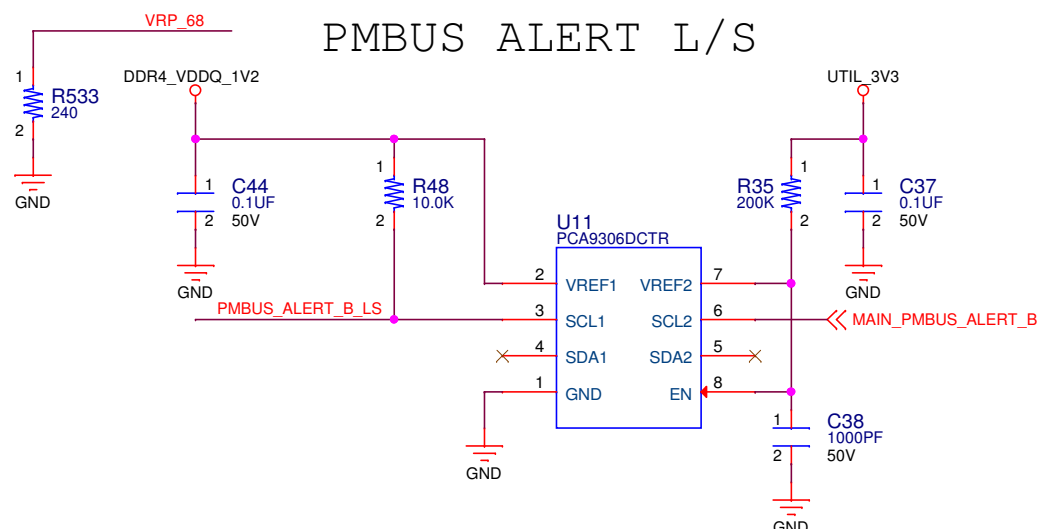
XCVU37PFSVH2892
BANK 69

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IO_L23P_T3U_N8_69_BE4
IO_L22N_T3U_N7_DBC_AD0N_69_BE5
IO_L22P_T3U_N6_DBC_AD0P_69_BE6
IO_L21N_T3L_N5_AD8N_69_BF2
IO_L21P_T3L_N4_AD8P_69_BF3
IO_L20N_T3L_N3_AD1N_69_BG2
IO_L20P_T3L_N2_AD1P_69_BG3
IO_L19N_T3L_N1_DBC_AD9N_69_BG4
IO_L19P_T3L_N0_DBC_AD9P_69_BG5
IO_T2U_N12_69_BF6
IO_L18N_T2U_N11_AD2N_69_BF7
IO_L18P_T2U_N10_AD2P_69_BF8
IO_L17N_T2U_N9_AD10N_69_BG7
IO_L17P_T2U_N8_AD10P_69_BG8
IO_L16N_T2U_N7_QBC_AD3N_69_BJ7
IO_L16P_T2U_N6_QBC_AD3P_69_BH7
IO_L15N_T2L_N5_AD11N_69_BK8
IO_L15P_T2L_N4_AD11P_69_BJ8
IO_L14N_T2L_N3_GC_69_BH4
IO_L14P_T2L_N2_GC_69_BH5
IO_L13N_T2L_N1_GC_QBC_69_BJ6
IO_L13P_T2L_N0_GC_QBC_69_BH6
IO_T1U_N12_69_BK6
IO_L12N_T1U_N11_GC_69_BK4
IO_L12P_T1U_N10_GC_69_BK5
IO_L11N_T1U_N9_GC_69_BK3
IO_L11P_T1U_N8_GC_69_BJ4
IO_L10N_T1U_N7_QBC_AD4N_69_BJ2
IO_L10P_T1U_N6_QBC_AD4P_69_BJ3
IO_L9N_T1L_N5_AD12N_69_BH1
IO_L9P_T1L_N4_AD12P_69_BH2
IO_L8N_T1L_N3_AD5N_69_BK1
IO_L8P_T1L_N2_AD5P_69_BJ1
IO_L7N_T1L_N1_QBC_AD13N_69_BL2
IO_L7P_T1L_N0_QBC_AD13P_69_BL3
IO_T0U_N12_VRP_69_BL5
IO_L6N_T0U_N11_AD6N_69_BM3
IO_L6P_T0U_N10_AD6P_69_BM4
IO_L5N_T0U_N9_AD14N_69_BM5
IO_L5P_T0U_N8_AD14P_69_BL6
IO_L4N_T0U_N7_DBC_AD7N_69_BM7
IO_L4P_T0U_N6_DBC_AD7P_69_BL7
IO_L3N_T0L_N5_AD15N_69_BN4
IO_L3P_T0L_N4_AD15P_69_BN5
IO_L2N_T0L_N3_69_BN6
IO_L2P_T0L_N2_69_BN7
IO_L1N_T0L_N1_DBC_69_BP6
IO_L1P_T0L_N0_DBC_69_BP7
VREF_69_BE8

BF5 QDR4_A0
BF1 QDR4_A1
BE1 QDR4_A2
BE3 QDR4_A3
BE4 QDR4_A4
BE5 QDR4_A5
BE6 QDR4_A6
BF2 QDR4_A7
BF3 QDR4_A8
BG2 QDR4_A9
BG3 QDR4_A10
BG4 QDR4_A11
BG5 QDR4_A12
BF6
BF7
BF8 QDR4_A13
BG7 QDR4_A14
BG8 QDR4_A15
BJ7 QDR4_A16
BH7 QDR4_A17
BK8 QDR4_A18
BJ8 QDR4_A19
BH4 QDR4_A20
BH5 QDR4_CK_N
BJ6 QDR4_CK_P
BH6 QDR4_A21
BK6 QDR4_A23
BK4 QDR4_AP
BK5 QDR4_A24
BK3 QDR4_A22
BJ4 QDR4_CLK_100MHZ_N
BJ2 QDR4_CLK_100MHZ_P
BJ3 QDR4_PE_N
BH1 QDR4_LBK0_N
BH2 QDR4_LBK1_N
BK1 QDR4_CFG_N
BJ1 QDR4_RST_N
BL2 QDR4_AINV
BL3 QDR4_LDB_N
BL5 VRP_69 QDR4_RWB_N
BM3
BM4 QDR4_LDA_N
BM5 QDR4_RWA_N
BL6 QSFPP3_MODSKLL_LS
BM7 QSFPP3_RESETL_LS
BL7 QSFPP3_MODPRSL_LS
BN4 QSFPP3_INTL_LS
BN5 QSFPP3_LPMODE_LS
BN6 QSFPP2_MODSKLL_LS
BN7 QSFPP2_RESETL_LS
BP6 QSFPP2_MODPRSL_LS
BP7 QSFPP2_INTL_LS
BE8 QSFPP2_LPMODE_LS

QDR4_VDDQ_1V2
BG6
BH3
BK7
VCCO_69_BG6
VCCO_69_BH3
VCCO_69_BK7
VREF_69_BE8

FPGA-XCVU37P-H2892



		PCB P/N : 1281016 ASSY P/N : 0432120 TEST P/N : TSS0201	
Title: HW-U1-VCU128 006 FPGA Bank 68 69			
Size B	Date Modified: Wednesday, October 10, 2018	Document Number: 0381852	Ver 1.0 Rev 01
Engineer: RO		Sheet 6 of 69	

U1-33

XCVU37PFSVH2892
BANK 70

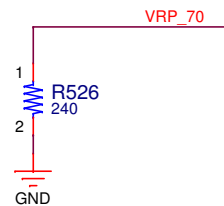
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IO_L24N_T3U_N11_70_A8
IO_L24P_T3U_N10_70_A9
IO_L23N_T3U_N9_70_A10
IO_L23P_T3U_N8_70_A11
IO_L22N_T3U_N7_DBC_AD0N_70_A13
IO_L22P_T3U_N6_DBC_AD0P_70_B13
IO_L21N_T3L_N5_AD8N_70_B12
IO_L21P_T3L_N4_AD8P_70_C12
IO_L20N_T3L_N3_AD1N_70_B10
IO_L20P_T3L_N2_AD1P_70_B11
IO_L19N_T3L_N1_DBC_AD9N_70_C9
IO_L19P_T3L_N0_DBC_AD9P_70_C10
IO_T2U_N12_70_C14
IO_L18N_T2U_N11_AD2N_70_A14
IO_L18P_T2U_N10_AD2P_70_A15
IO_L17N_T2U_N9_AD10N_70_B15
IO_L17P_T2U_N8_AD10P_70_C15
IO_L16N_T2U_N7_QBC_AD3N_70_D14
IO_L16P_T2U_N6_QBC_AD3P_70_D15
IO_L15N_T2L_N5_AD11N_70_E14
IO_L15P_T2L_N4_AD11P_70_F15
IO_L14N_T2L_N3_GC_70_F13
IO_L14P_T2L_N2_GC_70_F14
IO_L13N_T2L_N1_GC_QBC_70_D12
IO_L13P_T2L_N0_GC_QBC_70_E13
IO_T1U_N12_70_H9
IO_L12N_T1U_N11_GC_70_E11
IO_L12P_T1U_N10_GC_70_F11
IO_L11N_T1U_N9_GC_70_D11
IO_L11P_T1U_N8_GC_70_E12
IO_L10N_T1U_N7_QBC_AD4N_70_D9
IO_L10P_T1U_N6_QBC_AD4P_70_D10
IO_L9N_T1L_N5_AD12N_70_E9
IO_L9P_T1L_N4_AD12P_70_F9
IO_L8N_T1L_N3_AD5N_70_F10
IO_L8P_T1L_N2_AD5P_70_G11
IO_L7N_T1L_N1_QBC_AD13N_70_G10
IO_L7P_T1L_N0_QBC_AD13P_70_H10
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IO_L6N_T0U_N11_AD6N_70_G13
IO_L6P_T0U_N10_AD6P_70_H14
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IO_L4P_T0U_N6_DBC_AD7P_70_H15
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IO_L2P_T0L_N2_70_J15
IO_L1N_T0L_N1_DBC_70_K13
IO_L1P_T0L_N0_DBC_70_K14

C13
A8
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A11
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B13
B12
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F15
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E9
F9
F10
G11
G10
H10
G12
G13
H14
H12
H13
G15
H15
J11
J12
J14
J15
K13
K14
L15

QDR4_DQB31
QDR4_DQB32
QDR4_DQB35
QDR4_DQB28
QDR4_DQB29
QDR4_DQB30
QDR4_DQB27
QDR4_DQB34
QDR4_DQB33
QDR4_DKB1_N
QDR4_DKB1_P
QDR4_DQB19
QDR4_DQB25
QDR4_DQB21
QDR4_DQB23
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QDR4_DQB20
QDR4_DQB18
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QDR4_QKB1_P
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QDR4_DQB16
QDR4_DQB17
QDR4_DQB10
QDR4_QVLDB0
QDR4_DQB13
QDR4_DQB14
QDR4_DQB15
QDR4_DQB11
QDR4_DQB9
QDR4_QKB0_N
QDR4_QKB0_P
QDR4_DQB5
QDR4_DQB4
QDR4_DQB7
QDR4_DQB8
QDR4_DQB0
QDR4_DQB3
QDR4_DQB2
QDR4_DQB6
QDR4_DQB1
QDR4_DKB0_N
QDR4_DKB0_P

QDR4_VDDQ_1V2
G14
H11
K15
VCCO_70_G14
VCCO_70_H11
VCCO_70_K15
VRP_70

FPGA-XCVU37P-H2892



U1-34

XCVU37PFSVH2892
BANK 71

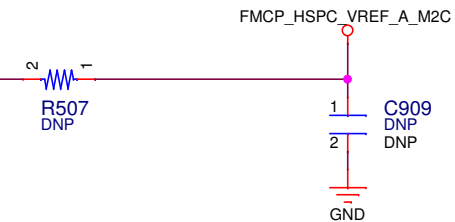
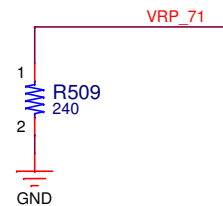
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IO_L23P_T3U_N8_71_A19
IO_L22N_T3U_N7_DBC_AD0N_71_A20
IO_L22P_T3U_N6_DBC_AD0P_71_A21
IO_L21N_T3L_N5_AD8N_71_B17
IO_L21P_T3L_N4_AD8P_71_B18
IO_L20N_T3L_N3_AD1N_71_B20
IO_L20P_T3L_N2_AD1P_71_B21
IO_L19N_T3L_N1_DBC_AD9N_71_C17
IO_L19P_T3L_N0_DBC_AD9P_71_C18
IO_T2U_N12_71_C20
IO_L18N_T2U_N11_AD2N_71_D19
IO_L18P_T2U_N10_AD2P_71_D20
IO_L17N_T2U_N9_AD10N_71_D16
IO_L17P_T2U_N8_AD10P_71_D17
IO_L16N_T2U_N7_QBC_AD3N_71_D21
IO_L16P_T2U_N6_QBC_AD3P_71_E21
IO_L15N_T2L_N5_AD11N_71_E16
IO_L15P_T2L_N4_AD11P_71_F16
IO_L14N_T2L_N3_GC_71_E18
IO_L14P_T2L_N2_GC_71_E19
IO_L13N_T2L_N1_GC_QBC_71_E17
IO_L13P_T2L_N0_GC_QBC_71_F18
IO_T1U_N12_71_J16
IO_L12N_T1U_N11_GC_71_F19
IO_L12P_T1U_N10_GC_71_F20
IO_L11N_T1U_N9_GC_71_G17
IO_L11P_T1U_N8_GC_71_G18
IO_L10N_T1U_N7_QBC_AD4N_71_F21
IO_L10P_T1U_N6_QBC_AD4P_71_G21
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IO_L9P_T1L_N4_AD12P_71_H19
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IO_L8P_T1L_N2_AD5P_71_H20
IO_L7N_T1L_N1_QBC_AD13N_71_G16
IO_L7P_T1L_N0_QBC_AD13P_71_H17
IO_T0U_N12_VRP_71_J17
IO_L6N_T0U_N11_AD6N_71_J19
IO_L6P_T0U_N10_AD6P_71_J20
IO_L5N_T0U_N9_AD14N_71_J21
IO_L5P_T0U_N8_AD14P_71_K21
IO_L4N_T0U_N7_DBC_AD7N_71_K18
IO_L4P_T0U_N6_DBC_AD7P_71_K19
IO_L3N_T0L_N5_AD15N_71_L20
IO_L3P_T0L_N4_AD15P_71_L21
IO_L2N_T0L_N3_71_L18
IO_L2P_T0L_N2_71_L19
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IO_L1P_T0L_N0_DBC_71_K17

C19
A16
B16
A18
A19
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A21
B17
B18
B20
B21
C17
C18
C20
D19
D20
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K17
L16

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FMCP_HSPC_LA19_P
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FMCP_HSPC_LA17_CC_N
FMCP_HSPC_LA17_CC_P
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FMCP_HSPC_LA29_N
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FMCP_HSPC_LA32_N
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FMCP_HSPC_LA30_N
FMCP_HSPC_LA30_P
FMCP_HSPC_LA33_N
FMCP_HSPC_LA33_P

VADJ
F17
H21
J18
VCCO_71_F17
VCCO_71_H21
VCCO_71_J18
VRP_71

FPGA-XCVU37P-H2892



		PCB P/N : 1281016 ASSY P/N : 0432120 TEST P/N : TSS0201	
Title: HW-U1-VCU128 007 FPGA Banks 70 71			
Size	Date Modified:	Document Number:	Ver
B	Wednesday, October 10, 2018	0381852	1.0
Engineer: RO		Sheet 7 of 69	

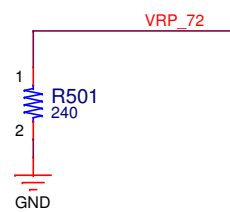
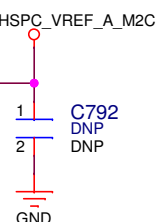
U1-35

XCVU37PFSVH2892
BANK 72

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IO_L23P_T3U_N8_72_B27
IO_L22N_T3U_N7_DBC_AD0N_72_A23
IO_L22P_T3U_N6_DBC_AD0P_72_B23
IO_L21N_T3L_N5_AD8N_72_B25
IO_L21P_T3L_N4_AD8P_72_B26
IO_L20N_T3L_N3_AD1N_72_C24
IO_L20P_T3L_N2_AD1P_72_C25
IO_L19N_T3L_N1_DBC_AD9N_72_B22
IO_L19P_T3L_N0_DBC_AD9P_72_C23
IO_T2U_N12_72_C27
IO_L18N_T2U_N11_AD2N_72_D27
IO_L18P_T2U_N10_AD2P_72_E27
IO_L17N_T2U_N9_AD10N_72_D26
IO_L17P_T2U_N8_AD10P_72_E26
IO_L16N_T2U_N7_QBC_AD3N_72_D24
IO_L16P_T2U_N6_QBC_AD3P_72_D25
IO_L15N_T2L_N5_AD11N_72_D22
IO_L15P_T2L_N4_AD11P_72_E22
IO_L14N_T2L_N3_GC_72_F25
IO_L14P_T2L_N2_GC_72_F26
IO_L13N_T2L_N1_GC_QBC_72_E23
IO_L13P_T2L_N0_GC_QBC_72_E24
IO_T1U_N12_72_H25
IO_L12N_T1U_N11_GC_72_G25
IO_L12P_T1U_N10_GC_72_G26
IO_L11N_T1U_N9_GC_72_F23
IO_L11P_T1U_N8_GC_72_F24
IO_L10N_T1U_N7_QBC_AD4N_72_G22
IO_L10P_T1U_N6_QBC_AD4P_72_G23
IO_L9N_T1L_N5_AD12N_72_G27
IO_L9P_T1L_N4_AD12P_72_H27
IO_L8N_T1L_N3_AD5N_72_H22
IO_L8P_T1L_N2_AD5P_72_J22
IO_L7N_T1L_N1_QBC_AD13N_72_H23
IO_L7P_T1L_N0_QBC_AD13P_72_H24
IO_T0U_N12_VRP_72_J24
IO_L6N_T0U_N11_AD6N_72_J25
IO_L6P_T0U_N10_AD6P_72_J26
IO_L5N_T0U_N9_AD14N_72_J27
IO_L5P_T0U_N8_AD14P_72_K27
IO_L4N_T0U_N7_DBC_AD7N_72_K22
IO_L4P_T0U_N6_DBC_AD7P_72_L23
IO_L3N_T0L_N5_AD15N_72_K23
IO_L3P_T0L_N4_AD15P_72_K24
IO_L2N_T0L_N3_72_K26
IO_L2P_T0L_N2_72_L26
IO_L1N_T0L_N1_DBC_72_L24
IO_L1P_T0L_N0_DBC_72_L25

C22
A24
A25
A26
B27
A23
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B26
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K23
K24
K26
L26
L24
L25
M23

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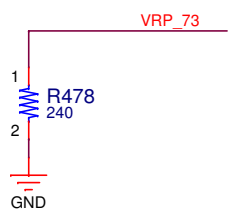
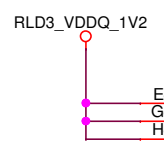
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XCVU37PFSVH2892
BANK 73

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IO_L24P_T3U_N10_73_A39
IO_L23N_T3U_N9_73_B42
IO_L23P_T3U_N8_73_B41
IO_L22N_T3U_N7_DBC_AD0N_73_A41
IO_L22P_T3U_N6_DBC_AD0P_73_B40
IO_L21N_T3L_N5_AD8N_73_D41
IO_L21P_T3L_N4_AD8P_73_E41
IO_L20N_T3L_N3_AD1N_73_C40
IO_L20P_T3L_N2_AD1P_73_D40
IO_L19N_T3L_N1_DBC_AD9N_73_F41
IO_L19P_T3L_N0_DBC_AD9P_73_F40
IO_T2U_N12_73_B43
IO_L18N_T2U_N11_AD2N_73_A44
IO_L18P_T2U_N10_AD2P_73_A43
IO_L17N_T2U_N9_AD10N_73_B45
IO_L17P_T2U_N8_AD10P_73_C44
IO_L16N_T2U_N7_QBC_AD3N_73_A46
IO_L16P_T2U_N6_QBC_AD3P_73_A45
IO_L15N_T2L_N5_AD11N_73_B46
IO_L15P_T2L_N4_AD11P_73_C45
IO_L14N_T2L_N3_GC_73_C43
IO_L14P_T2L_N2_GC_73_D42
IO_L13N_T2L_N1_GC_QBC_73_E43
IO_L13P_T2L_N0_GC_QBC_73_E42
IO_T1U_N12_73_G46
IO_L12N_T1U_N11_GC_73_D45
IO_L12P_T1U_N10_GC_73_D44
IO_L11N_T1U_N9_GC_73_E44
IO_L11P_T1U_N8_GC_73_F44
IO_L10N_T1U_N7_QBC_AD4N_73_D46
IO_L10P_T1U_N6_QBC_AD4P_73_E46
IO_L9N_T1L_N5_AD12N_73_G45
IO_L9P_T1L_N4_AD12P_73_H45
IO_L8N_T1L_N3_AD5N_73_F46
IO_L8P_T1L_N2_AD5P_73_F45
IO_L7N_T1L_N1_QBC_AD13N_73_H44
IO_L7P_T1L_N0_QBC_AD13P_73_J44
IO_T0U_N12_VRP_73_F43
IO_L6N_T0U_N11_AD6N_73_G43
IO_L6P_T0U_N10_AD6P_73_H43
IO_L5N_T0U_N9_AD14N_73_G42
IO_L5P_T0U_N8_AD14P_73_G41
IO_L4N_T0U_N7_DBC_AD7N_73_G40
IO_L4P_T0U_N6_DBC_AD7P_73_H40
IO_L3N_T0L_N5_AD15N_73_J41
IO_L3P_T0L_N4_AD15P_73_J40
IO_L2N_T0L_N3_73_H42
IO_L2P_T0L_N2_73_J42
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IO_L1P_T0L_N0_DBC_73_K41

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Title: HW-U1-VCU128 008 FPGA Banks 72 73			
Size	Date Modified:	Document Number:	Ver
B	Wednesday, October 10, 2018	0381852	1.0
Engineer: RO		Sheet 8 of 69	

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XCVU37PFSVH2892
BANK 74

IO_T3U_N12_74_C38
IO_L24N_T3U_N11_74_A35
IO_L24P_T3U_N10_74_A34
IO_L23N_T3U_N9_74_A36
IO_L23P_T3U_N8_74_B35
IO_L22N_T3U_N7_DBC_AD0N_74_A38
IO_L22P_T3U_N6_DBC_AD0P_74_B37
IO_L21N_T3L_N5_AD8N_74_B36
IO_L21P_T3L_N4_AD8P_74_C35
IO_L20N_T3L_N3_AD1N_74_B38
IO_L20P_T3L_N2_AD1P_74_C37
IO_L19N_T3L_N1_DBC_AD9N_74_C34
IO_L19P_T3L_N0_DBC_AD9P_74_D34
IO_T2U_N12_74_C39
IO_L18N_T2U_N11_AD2N_74_D37
IO_L18P_T2U_N10_AD2P_74_E36
IO_L17N_T2U_N9_AD10N_74_E34
IO_L17P_T2U_N8_AD10P_74_F34
IO_L16N_T2U_N7_QBC_AD3N_74_D39
IO_L16P_T2U_N6_QBC_AD3P_74_E39
IO_L15N_T2L_N5_AD11N_74_D36
IO_L15P_T2L_N4_AD11P_74_D35
IO_L14N_T2L_N3_GC_74_E38
IO_L14P_T2L_N2_GC_74_E37
IO_L13N_T2L_N1_GC_QBC_74_F36
IO_L13P_T2L_N0_GC_QBC_74_F35
IO_T1U_N12_74_J34
IO_L12N_T1U_N11_GC_74_F38
IO_L12P_T1U_N10_GC_74_G37
IO_L11N_T1U_N9_GC_74_G36
IO_L11P_T1U_N8_GC_74_G35
IO_L10N_T1U_N7_QBC_AD4N_74_F39
IO_L10P_T1U_N6_QBC_AD4P_74_G38
IO_L9N_T1L_N5_AD12N_74_H35
IO_L9P_T1L_N4_AD12P_74_H34
IO_L8N_T1L_N3_AD5N_74_H38
IO_L8P_T1L_N2_AD5P_74_H37
IO_L7N_T1L_N1_QBC_AD13N_74_H39
IO_L7P_T1L_N0_QBC_AD13P_74_J39
IO_T0U_N12_VRP_74_J35
IO_L6N_T0U_N11_AD6N_74_J37
IO_L6P_T0U_N10_AD6P_74_K37
IO_L5N_T0U_N9_AD14N_74_K34
IO_L5P_T0U_N8_AD14P_74_L34
IO_L4N_T0U_N7_DBC_AD7N_74_K38
IO_L4P_T0U_N6_DBC_AD7P_74_L38
IO_L3N_T0L_N5_AD15N_74_J36
IO_L3P_T0L_N4_AD15P_74_K36
IO_L2N_T0L_N3_74_K39
IO_L2P_T0L_N2_74_L39
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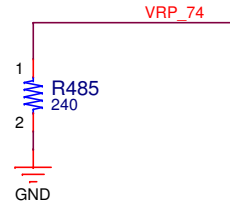
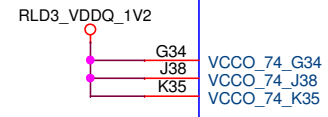
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M35

RLD3_72B_A6
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RLD3_72B_A0
RLD3_72B_A11
RLD3_72B_BA3
RLD3_72B_RESET_B
RLD3_72B_A15
RLD3_72B_A14
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RLD3_CLK_100MHZ_P
RLD3_72B_A3
RLD3_72B_CK_N
RLD3_72B_CK_P
RLD3_72B_DK3_N
RLD3_72B_DK3_P
RLD3_72B_DK2_N
RLD3_72B_DK2_P
RLD3_72B_DK1_N
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RLD3_72B_A9



U1-38

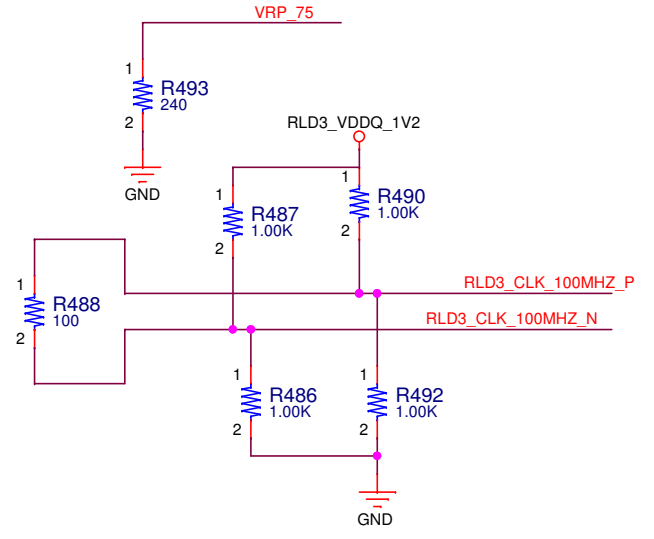
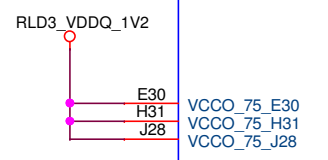
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IO_L23P_T3U_N8_75_A29
IO_L22N_T3U_N7_DBC_AD0N_75_A31
IO_L22P_T3U_N6_DBC_AD0P_75_B30
IO_L21N_T3L_N5_AD8N_75_A33
IO_L21P_T3L_N4_AD8P_75_B32
IO_L20N_T3L_N3_AD1N_75_C29
IO_L20P_T3L_N2_AD1P_75_C28
IO_L19N_T3L_N1_DBC_AD9N_75_B31
IO_L19P_T3L_N0_DBC_AD9P_75_C30
IO_T2U_N12_75_C33
IO_L18N_T2U_N11_AD2N_75_D29
IO_L18P_T2U_N10_AD2P_75_E28
IO_L17N_T2U_N9_AD10N_75_C32
IO_L17P_T2U_N8_AD10P_75_D32
IO_L16N_T2U_N7_QBC_AD3N_75_D31
IO_L16P_T2U_N6_QBC_AD3P_75_D30
IO_L15N_T2L_N5_AD11N_75_E33
IO_L15P_T2L_N4_AD11P_75_F33
IO_L14N_T2L_N3_GC_75_E29
IO_L14P_T2L_N2_GC_75_F29
IO_L13N_T2L_N1_GC_QBC_75_E32
IO_L13P_T2L_N0_GC_QBC_75_E31
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IO_L12N_T1U_N11_GC_75_F30
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IO_L11N_T1U_N9_GC_75_F31
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IO_L9N_T1L_N5_AD12N_75_G32
IO_L9P_T1L_N4_AD12P_75_H32
IO_L8N_T1L_N3_AD5N_75_H30
IO_L8P_T1L_N2_AD5P_75_H29
IO_L7N_T1L_N1_QBC_AD13N_75_G33
IO_L7P_T1L_N0_QBC_AD13P_75_H33
IO_T0U_N12_VRP_75_K28
IO_L6N_T0U_N11_AD6N_75_J29
IO_L6P_T0U_N10_AD6P_75_K29
IO_L5N_T0U_N9_AD14N_75_J31
IO_L5P_T0U_N8_AD14P_75_J30
IO_L4N_T0U_N7_DBC_AD7N_75_J32
IO_L4P_T0U_N6_DBC_AD7P_75_K32
IO_L3N_T0L_N5_AD15N_75_K31
IO_L3P_T0L_N4_AD15P_75_L31
IO_L2N_T0L_N3_75_L30
IO_L2P_T0L_N2_75_L29
IO_L1N_T0L_N1_DBC_75_K33
IO_L1P_T0L_N0_DBC_75_L33
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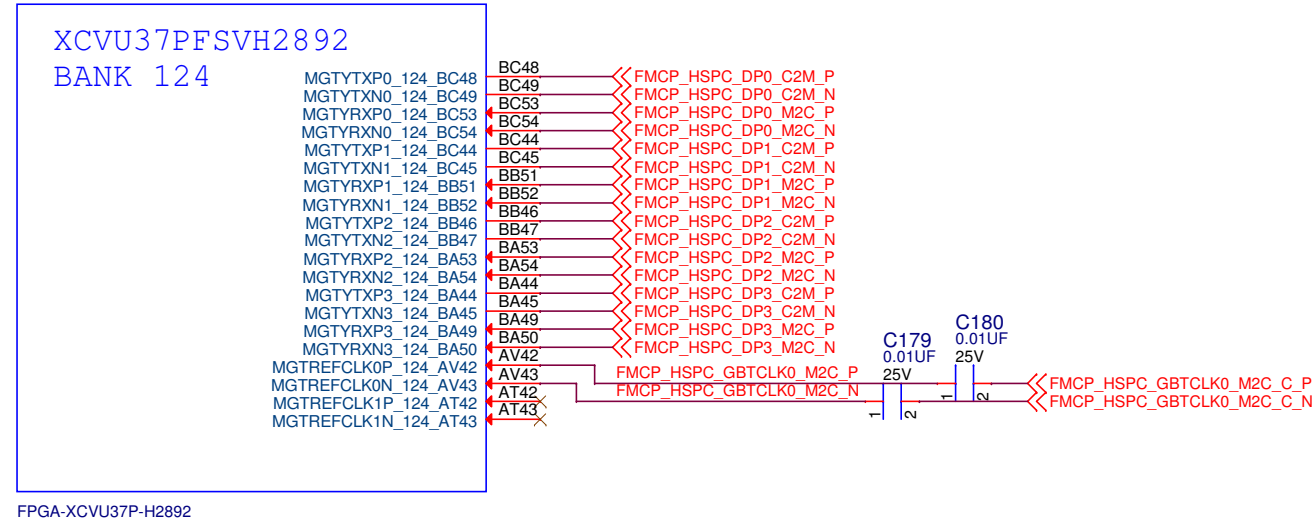
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RLD3_72B_DQ13
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RLD3_72B_QK1_P
RLD3_72B_DM0
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RLD3_72B_DQ3
RLD3_72B_DQ1
RLD3_72B_DQ7
RLD3_72B_DQ2
RLD3_72B_DQ8
RLD3_72B_DQ5
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VRP_75



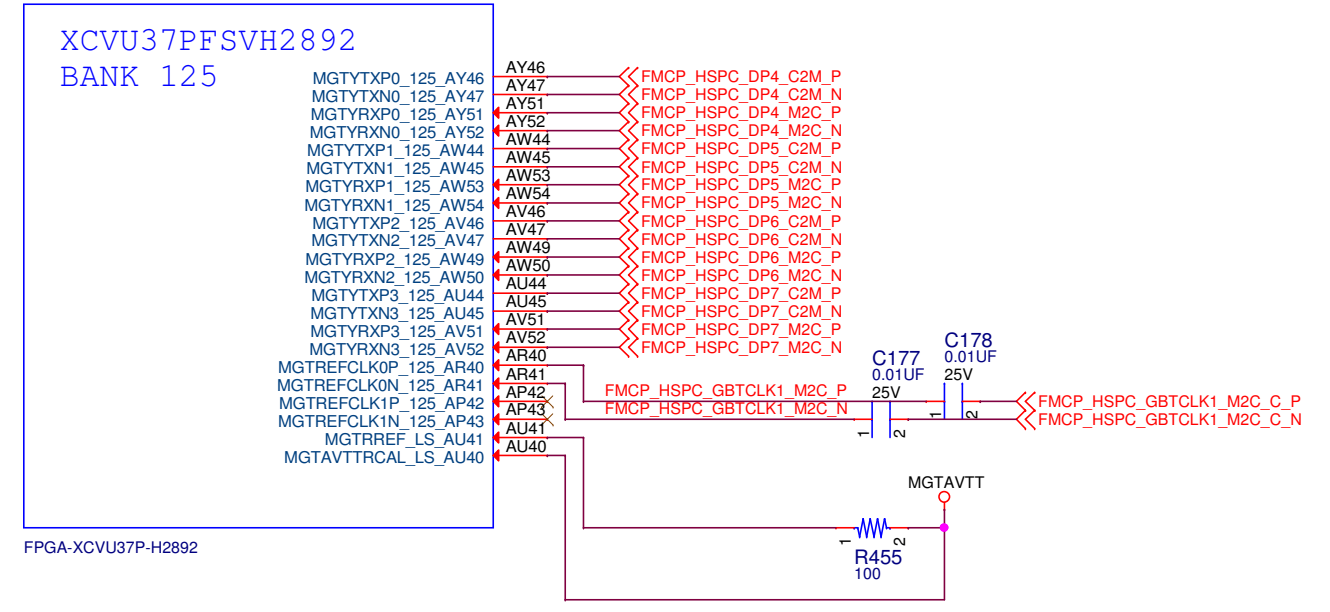
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Size	Date Modified:	Document Number:	Ver
B	Wednesday, October 10, 2018	0381852	1.0
Engineer: RO		Sheet 9 of 69	Rev 01

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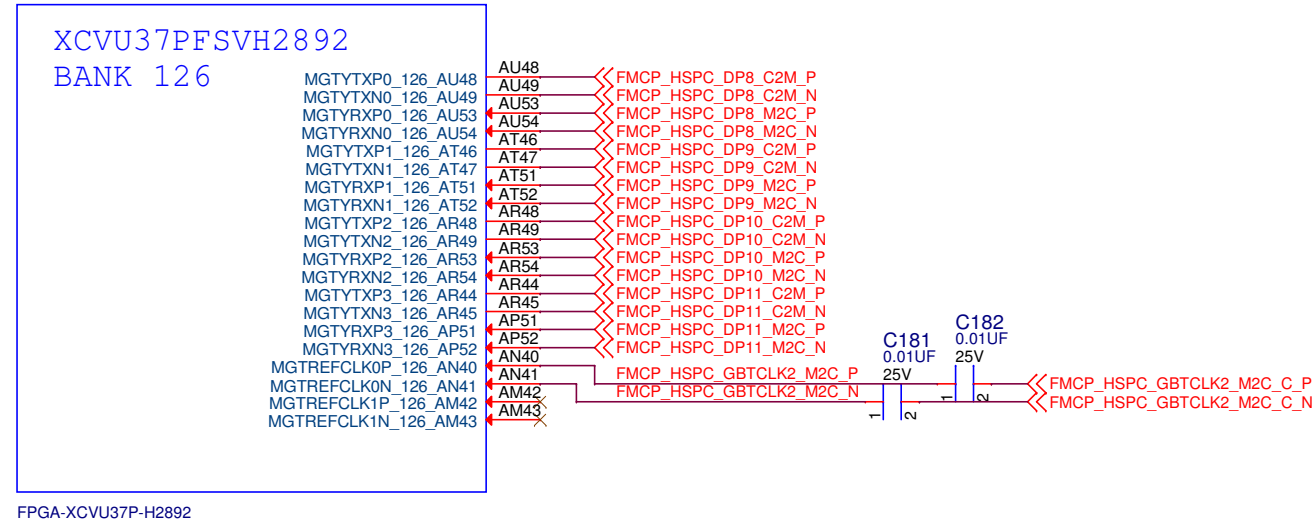
FPGA-XCVU37P-H2892

U1-3



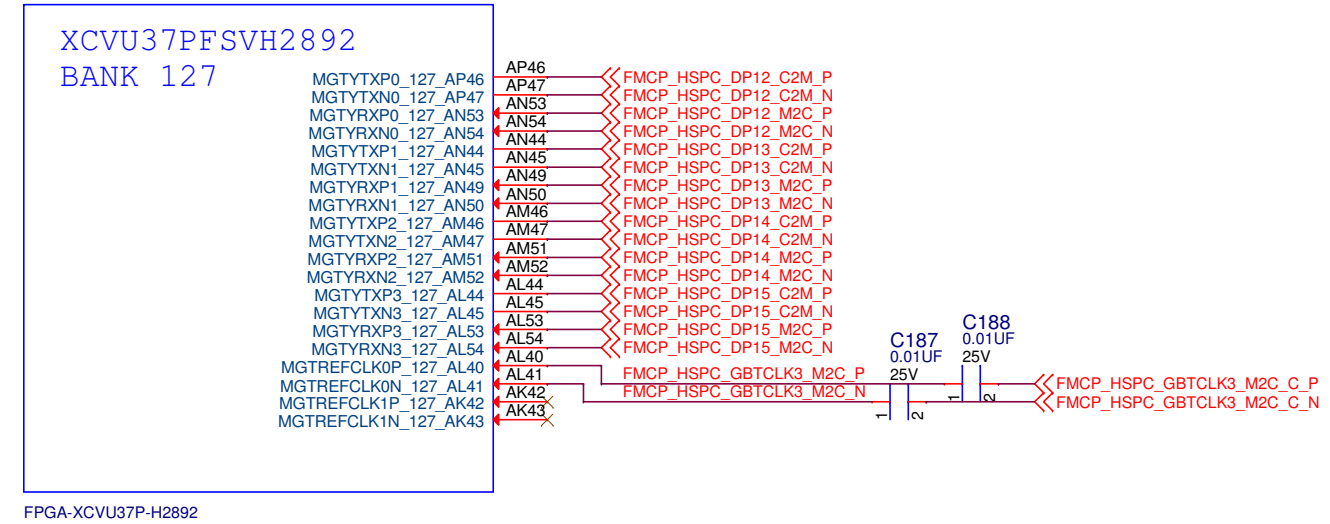
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U1-4



FPGA-XCVU37P-H2892

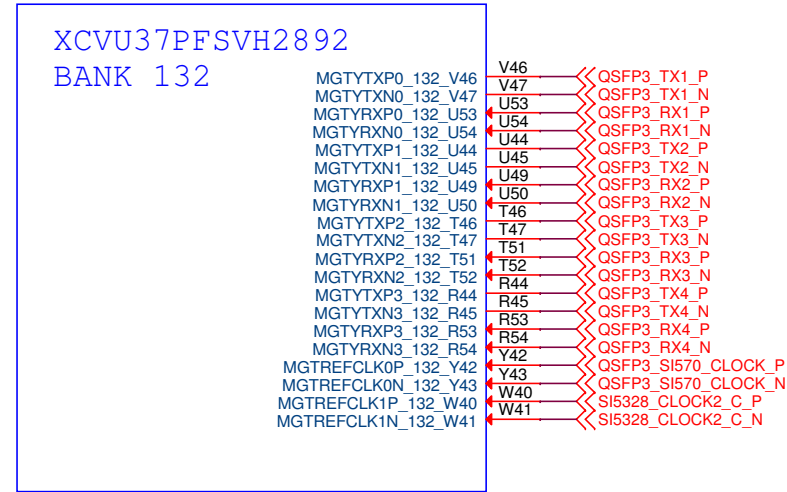
U1-5



FPGA-XCVU37P-H2892

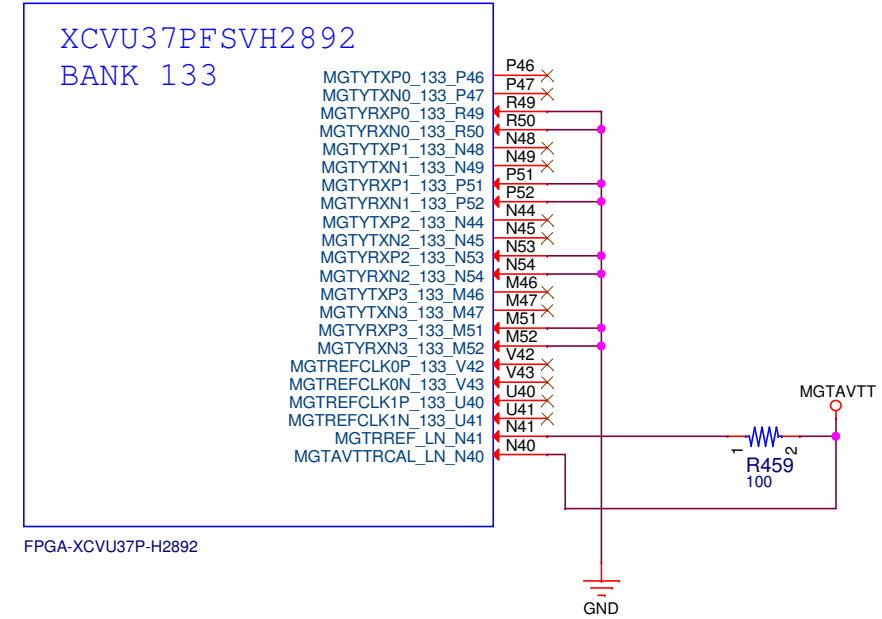
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Title: HW-U1-VCU128 011 FPGA Banks 124 125 126 127			
Size	Date Modified:	Document Number:	Ver
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U1-10



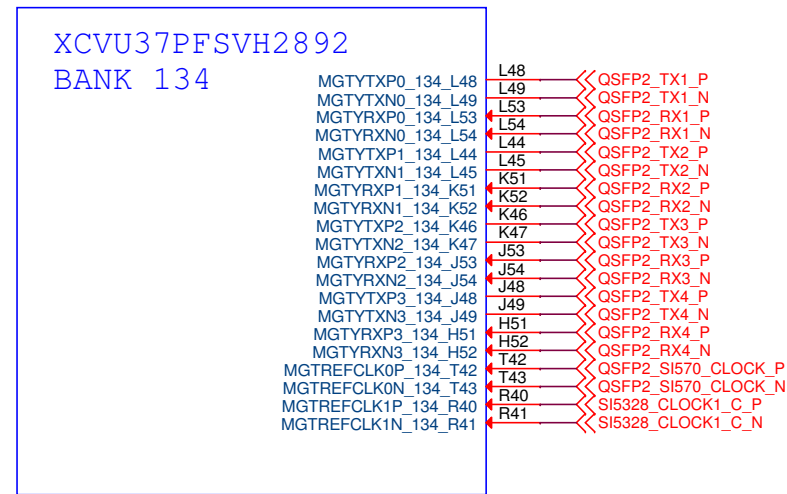
FPGA-XCVU37P-H2892

U1-11



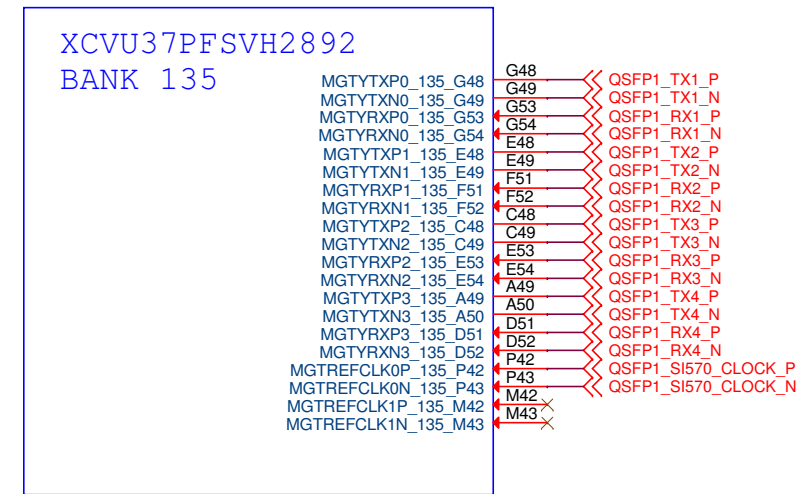
FPGA-XCVU37P-H2892

U1-12



FPGA-XCVU37P-H2892

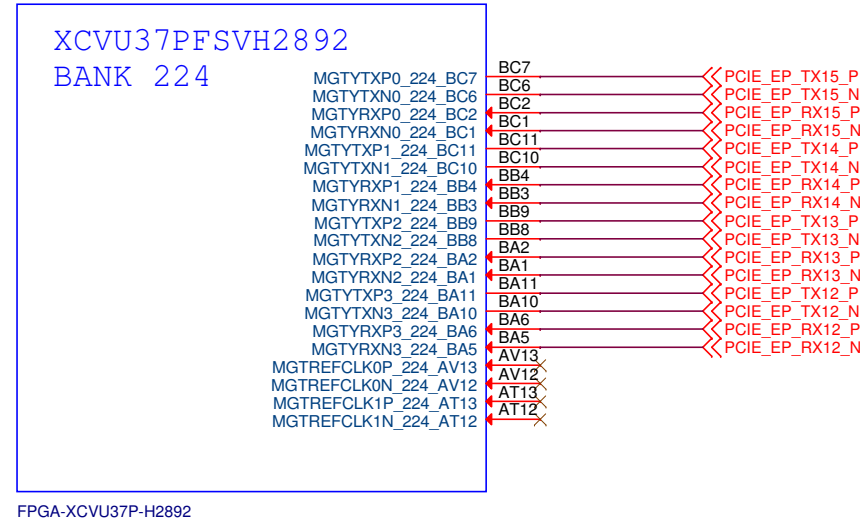
U1-13



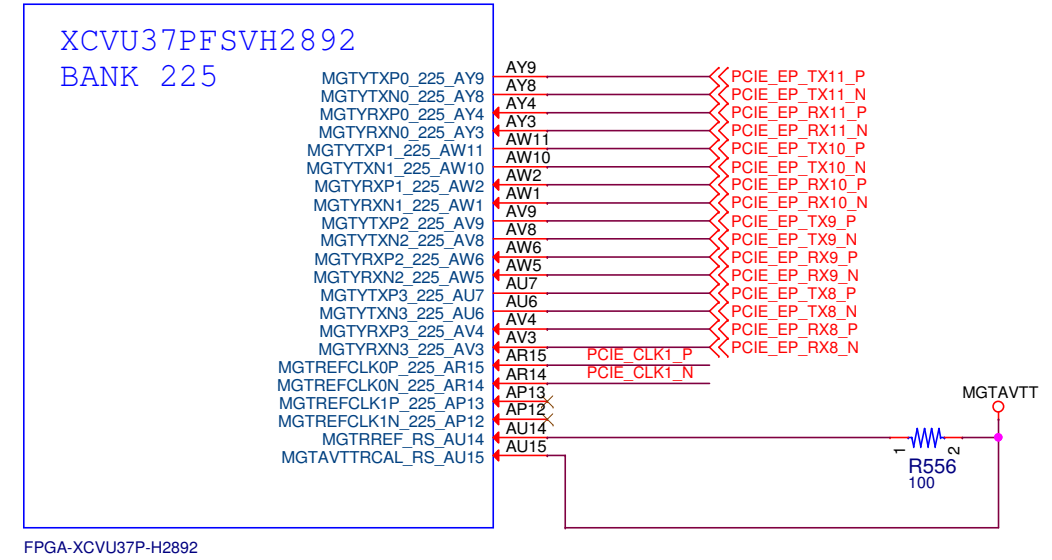
FPGA-XCVU37P-H2892

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Title: HW-U1-VCU128 013 FPGA Banks 132 133 134 135			
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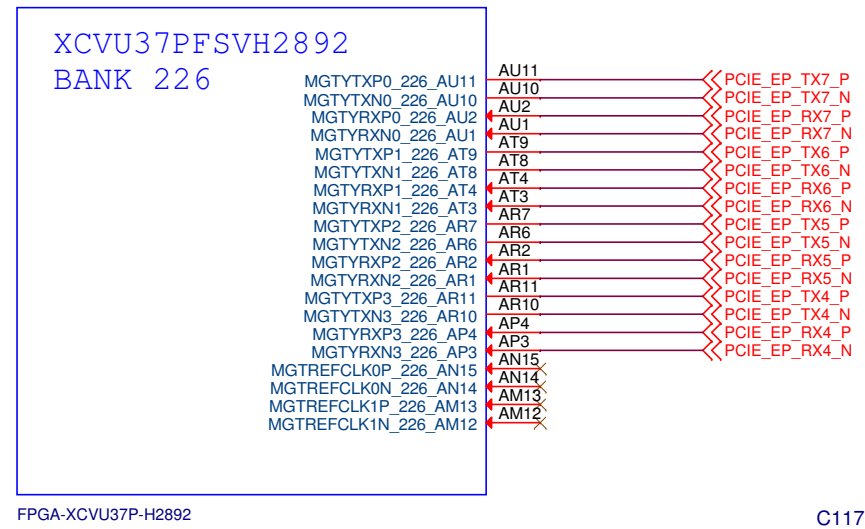
U1-14



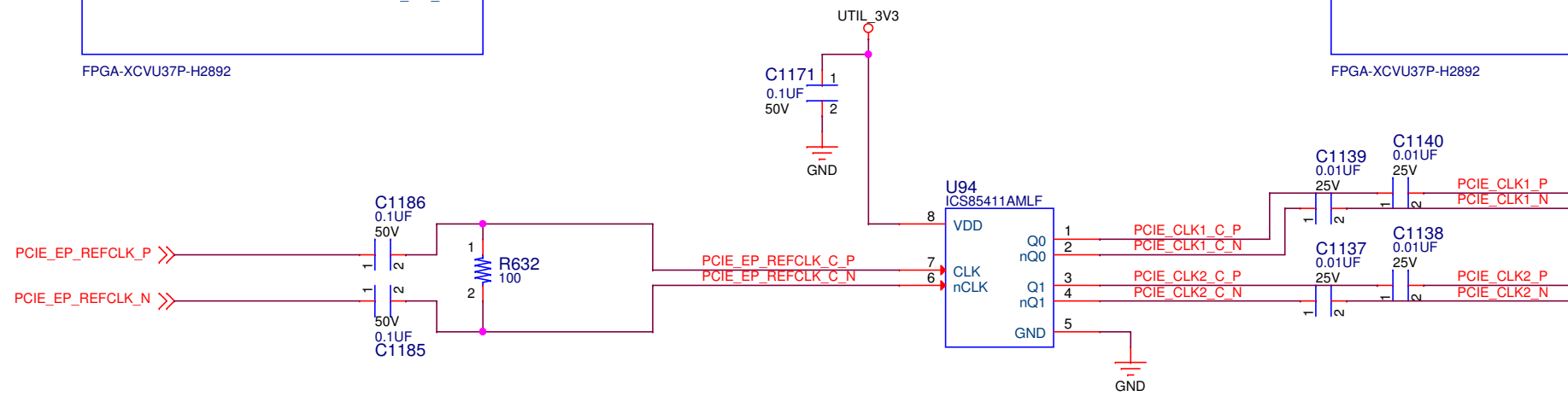
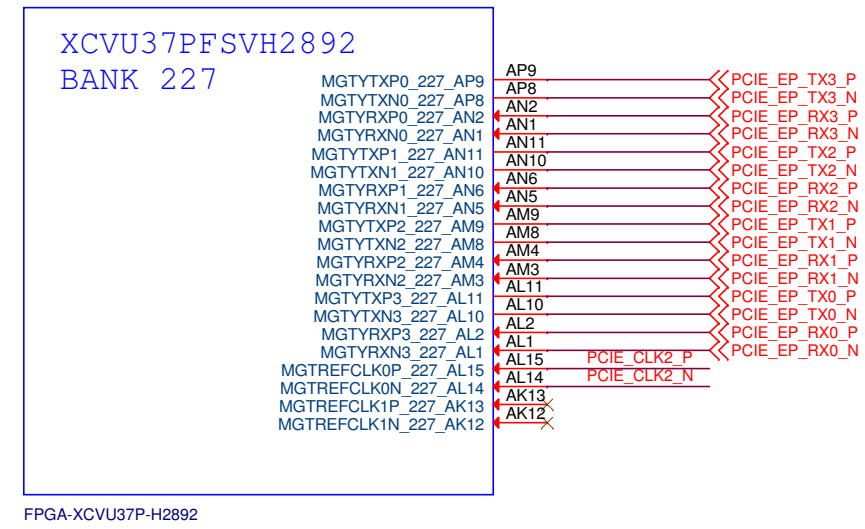
U1-15



U1-16

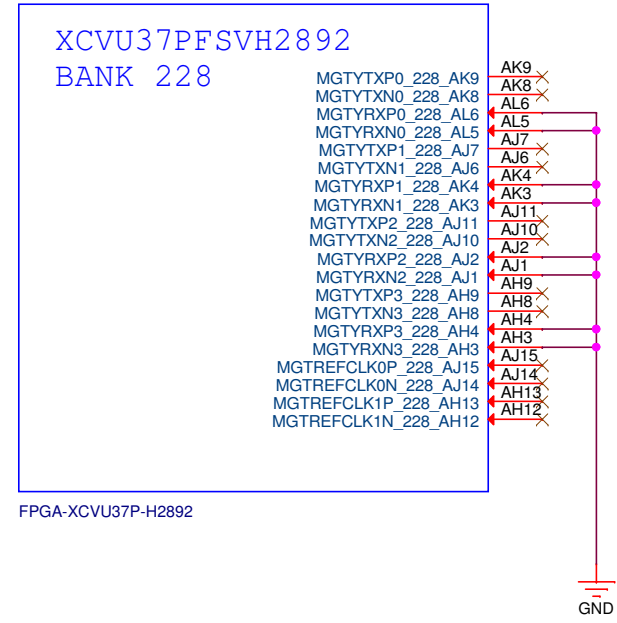


U1-17



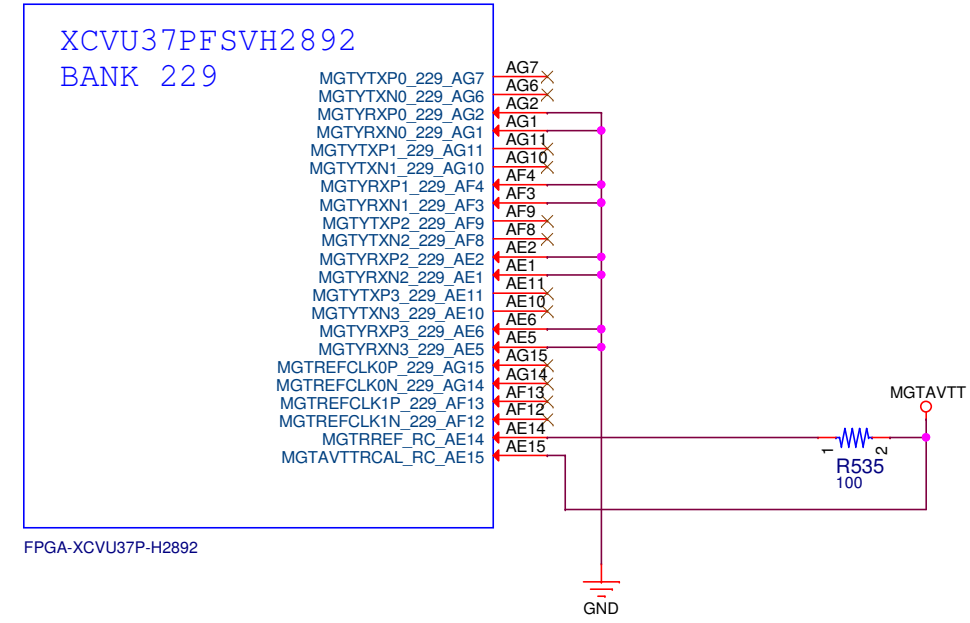
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Title: HW-U1-VCU128 014 FPGA Banks 224 225 226 227			
Size: B	Date Modified: Wednesday, October 10, 2018	Document Number: 0381852	Ver 1.0 Rev 01
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U1-18



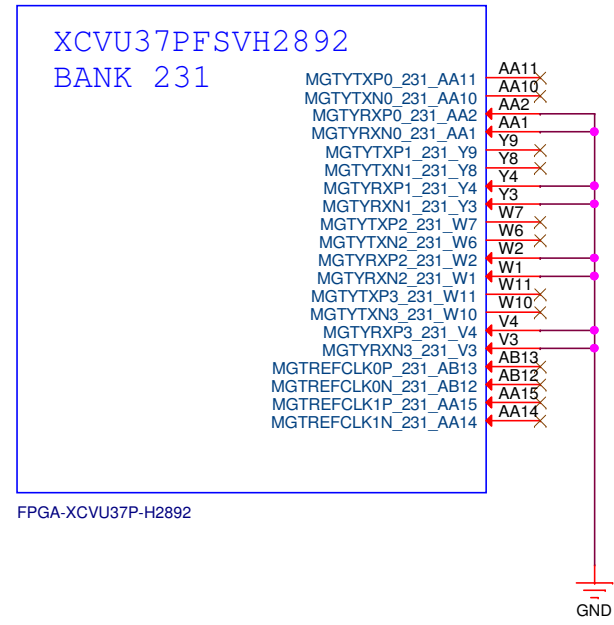
FPGA-XCVU37P-H2892

U1-19



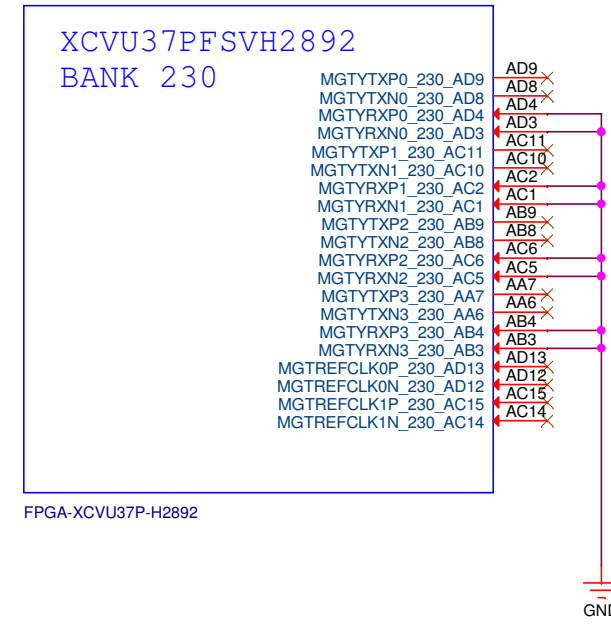
FPGA-XCVU37P-H2892

U1-21



FPGA-XCVU37P-H2892

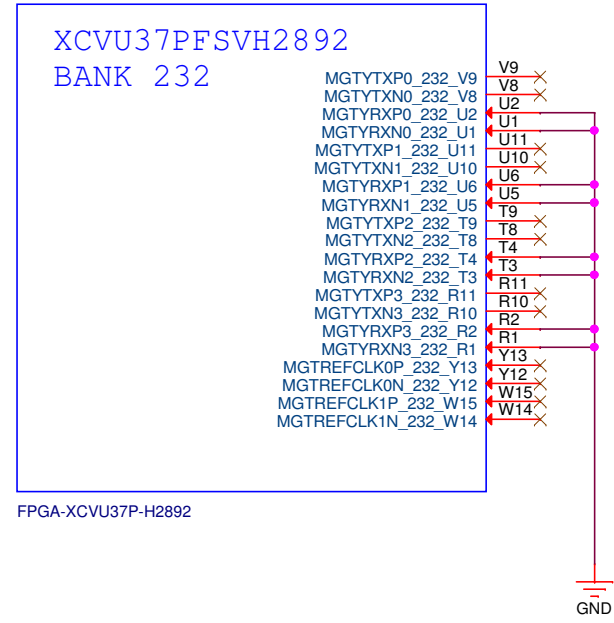
U1-20



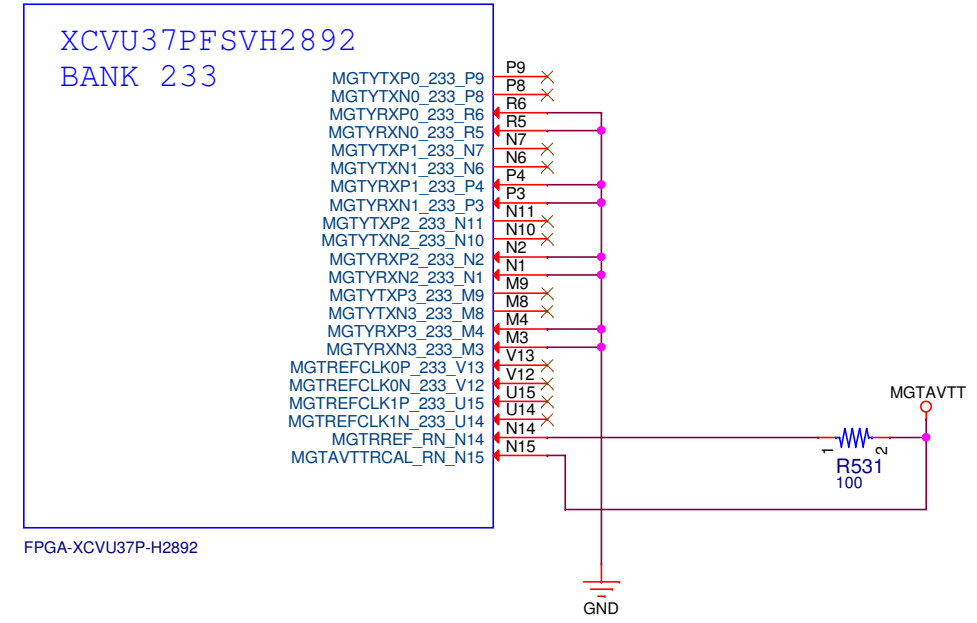
FPGA-XCVU37P-H2892

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Title: HW-U1-VCU128 015 FPGA Banks 228 229 230 231			
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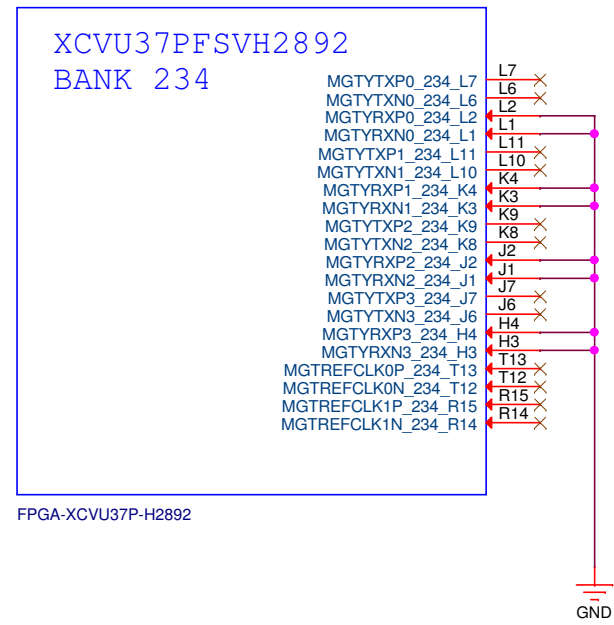
U1-22



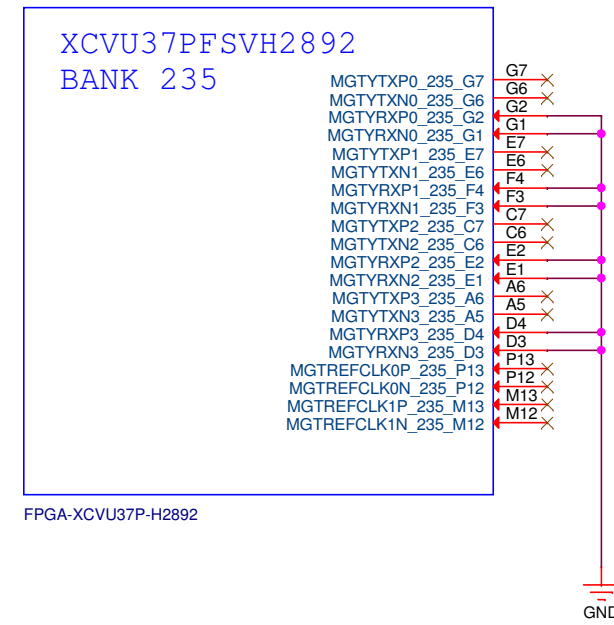
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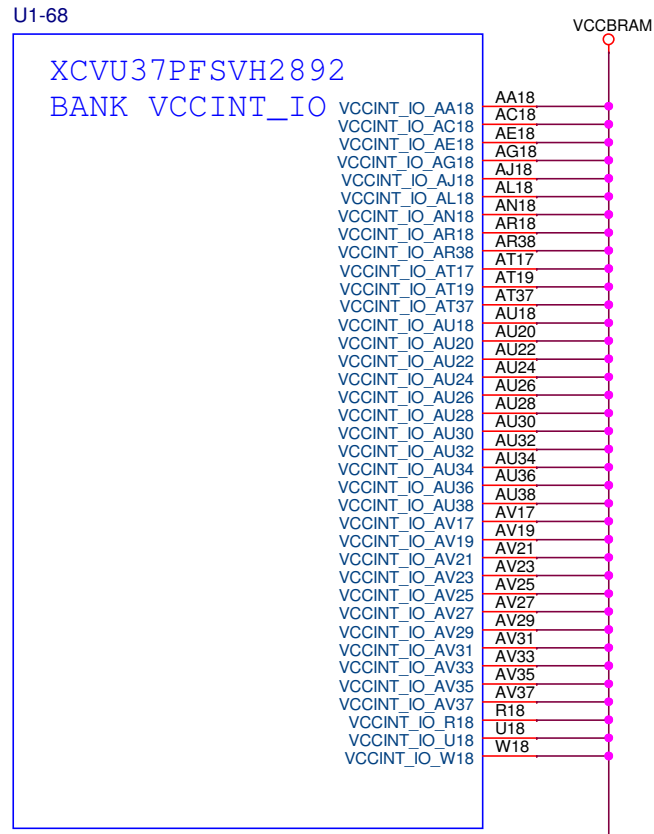
U1-24



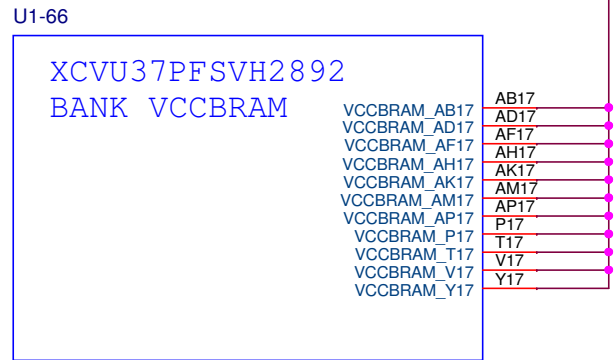
U1-25



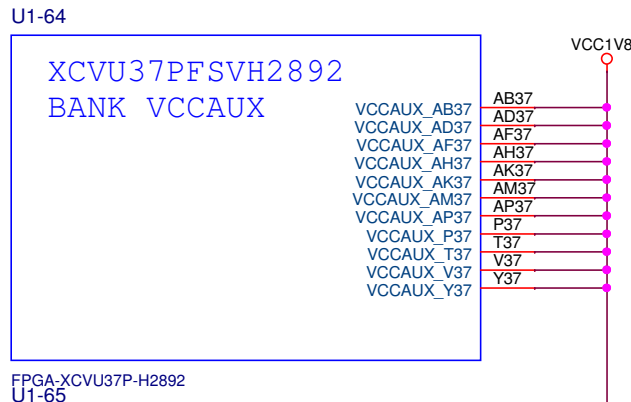
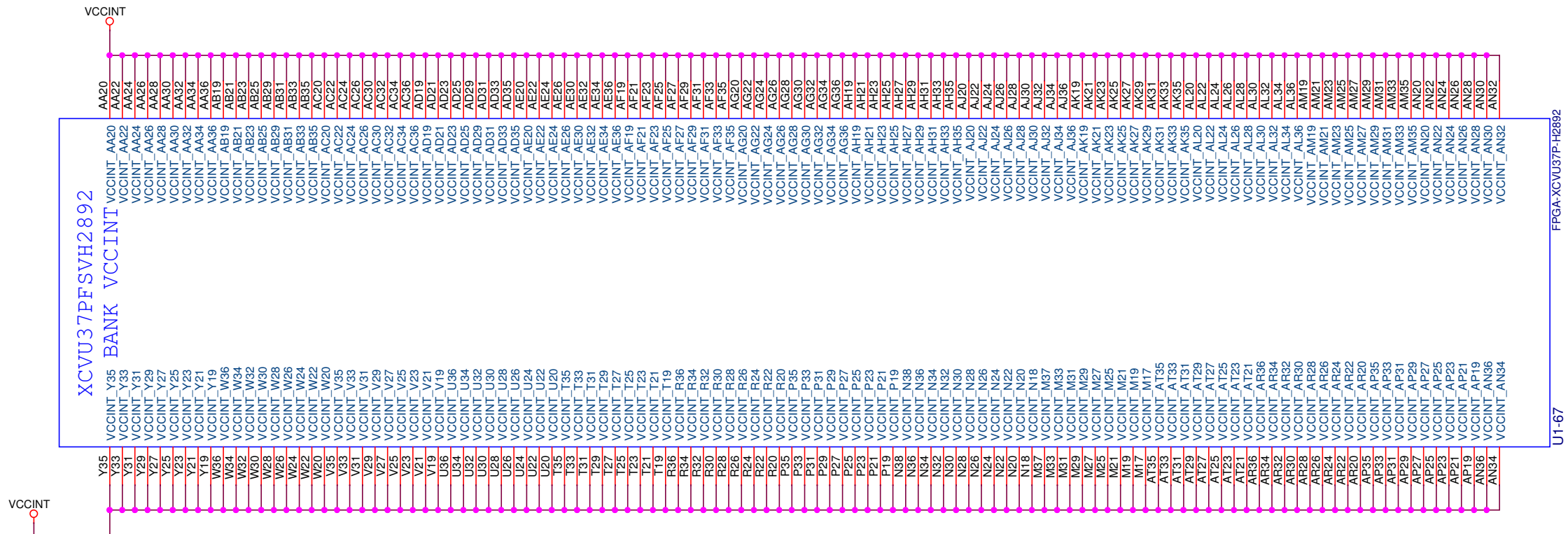
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Title: HW-U1-VCU128 016 FPGA Banks 232 233 234 235			
Size: B	Date Modified: Wednesday, October 10, 2018	Document Number: 0381852	Ver 1.0 Rev 01
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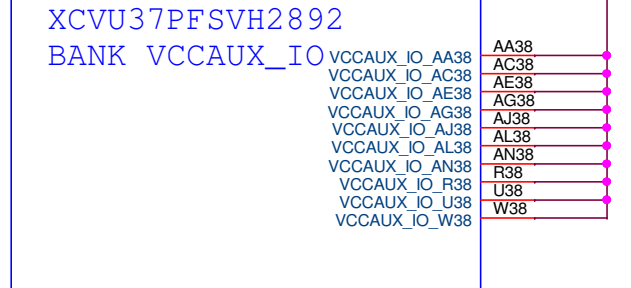


FPGA-XCVU37P-H2892

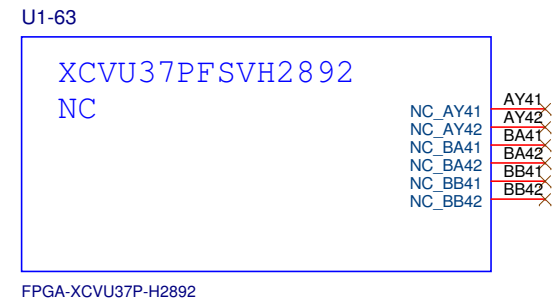


FPGA-XCVU37P-H2892

U1-65

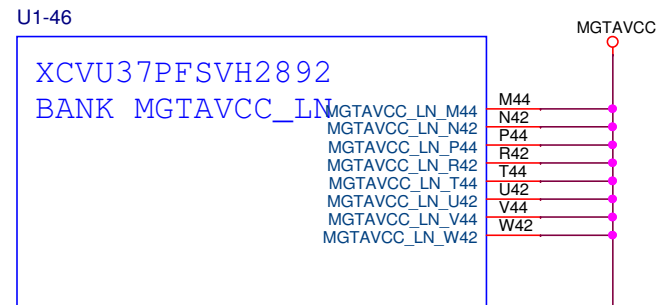


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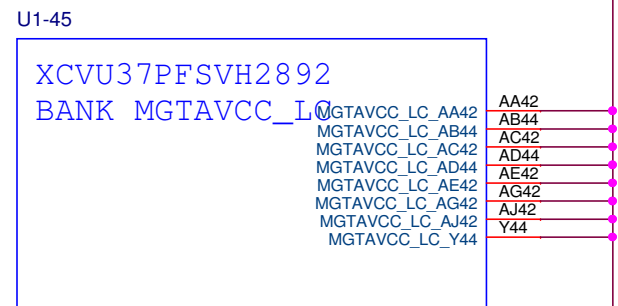


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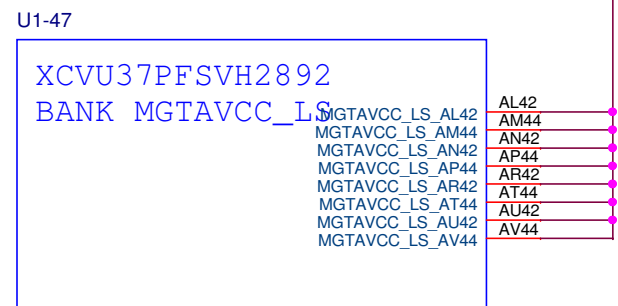
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Title: HW-U1-VCU128 017 FPGA Power 1		Ver 1.0	
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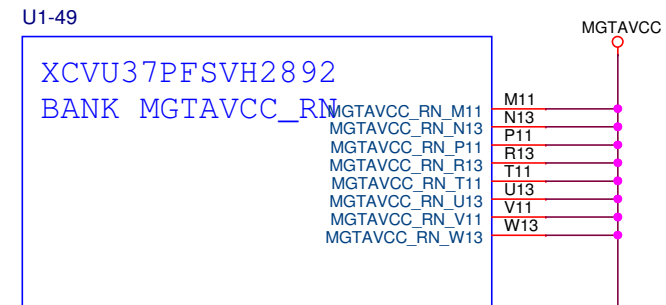
FPGA-XCVU37P-H2892



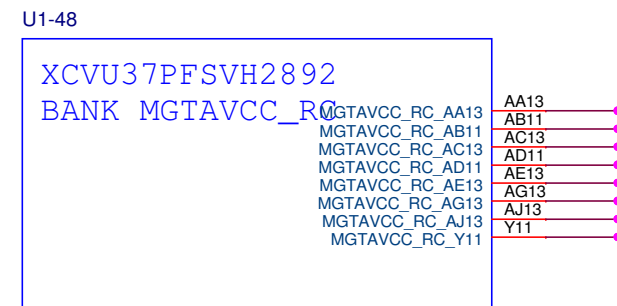
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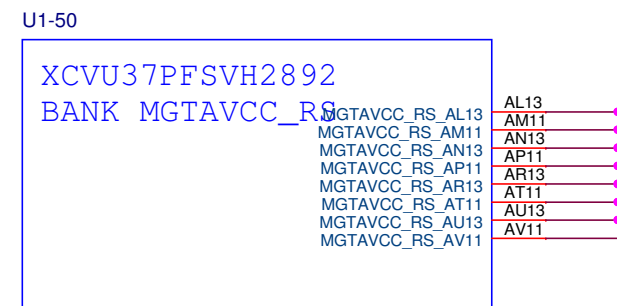
FPGA-XCVU37P-H2892



FPGA-XCVU37P-H2892

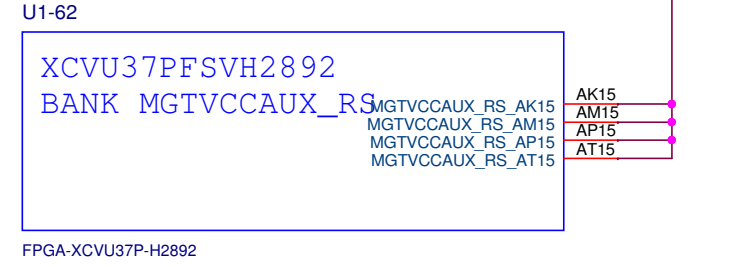
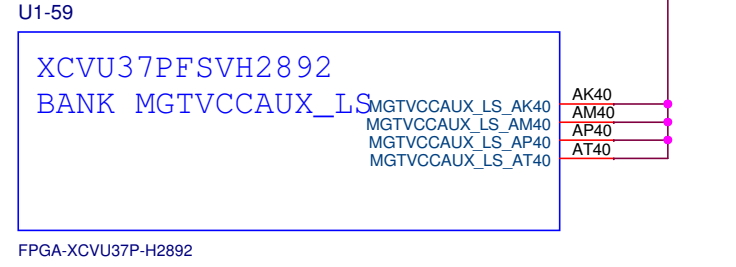
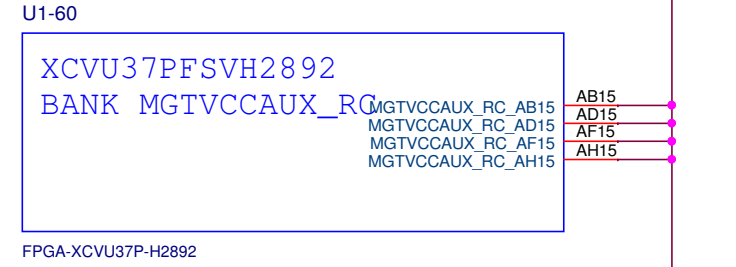
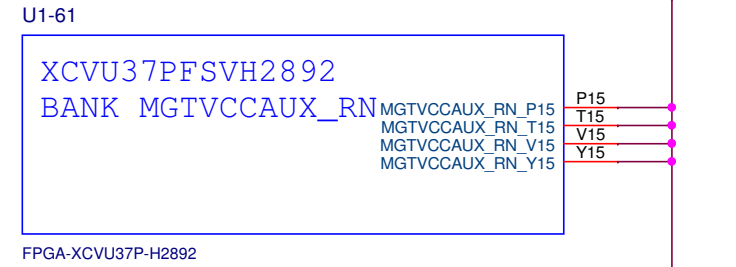
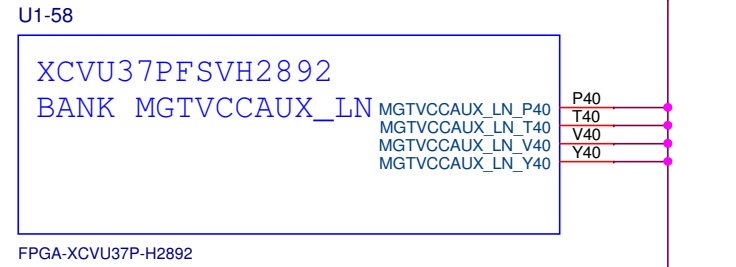
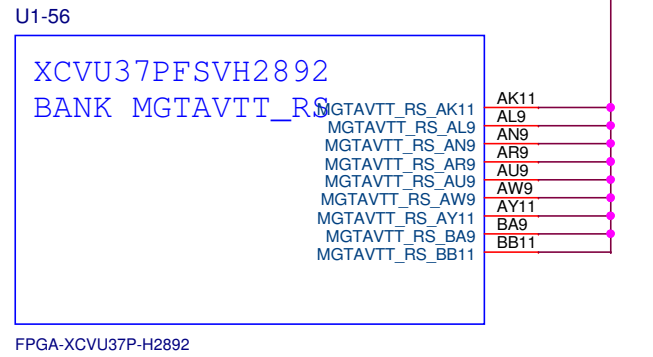
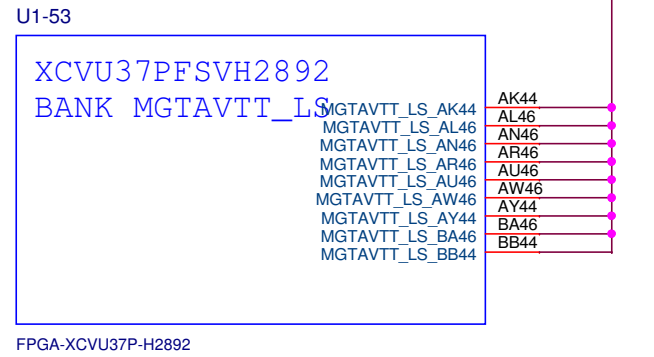
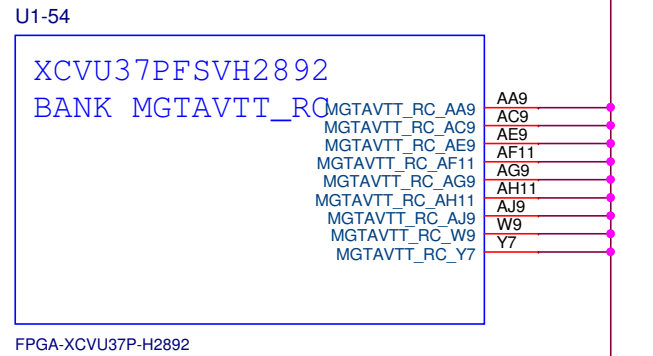
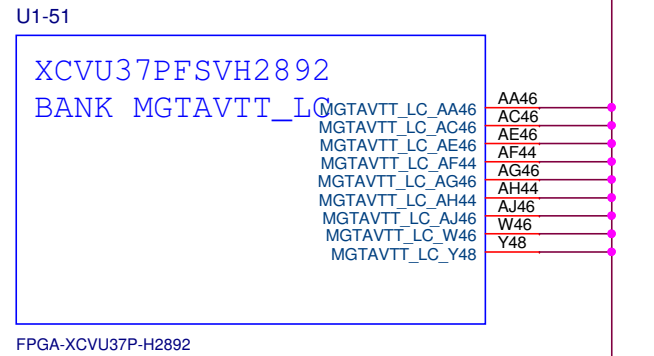
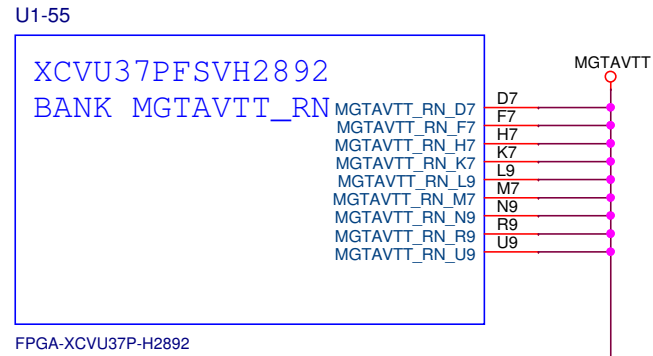
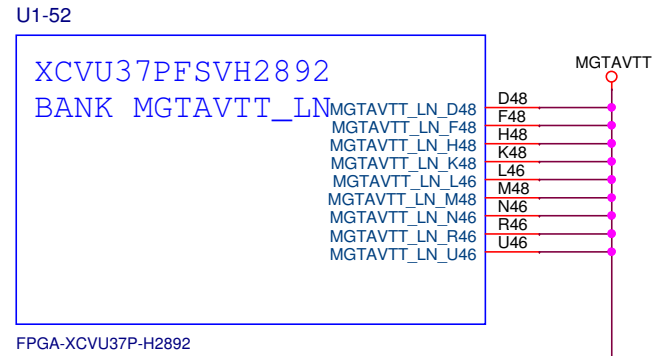



FPGA-XCVU37P-H2892

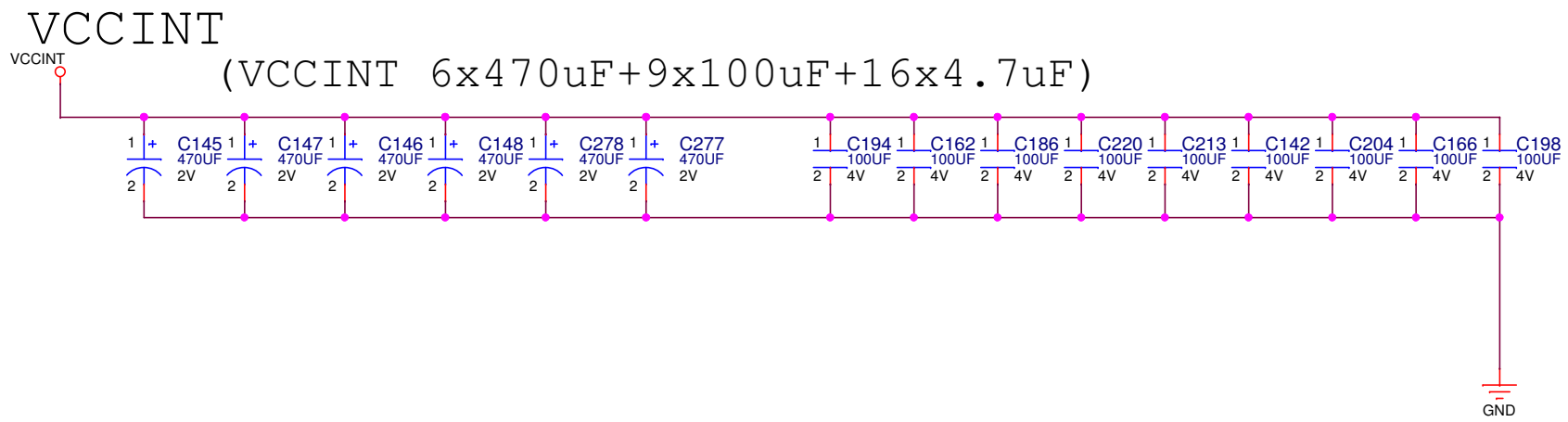


FPGA-XCVU37P-H2892

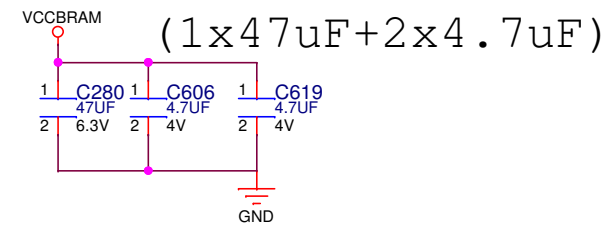
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Title: HW-U1-VCU128 018 FPGA Power 2			
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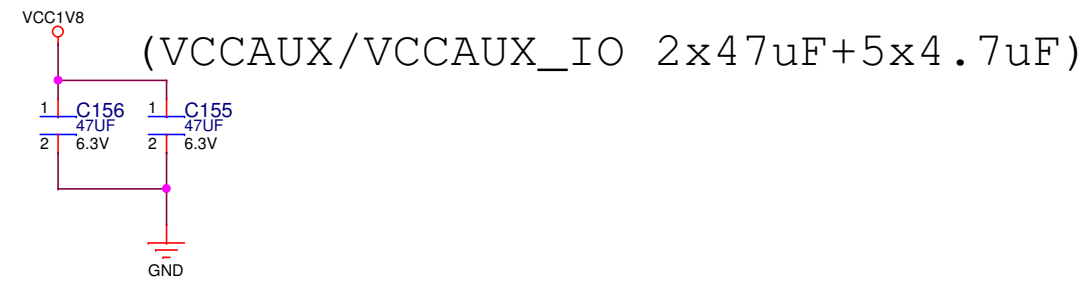
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Title: HW-U1-VCU128 019 FPGA Power 3			
Size	Date Modified:	Document Number:	Ver
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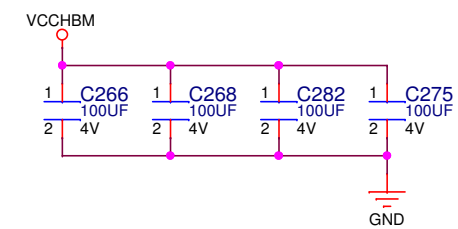
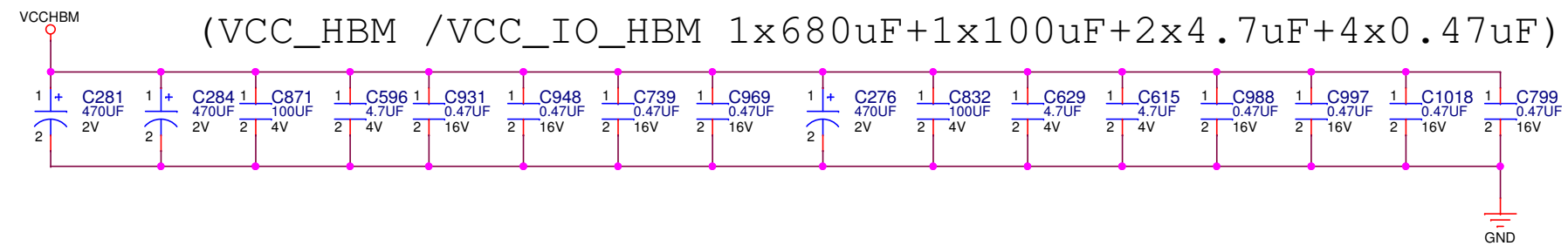
VCCBRAM/VCCINT_IO



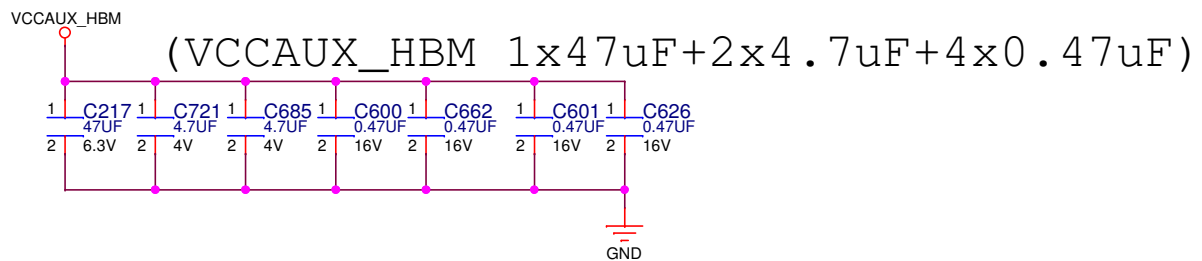
VCCAUX/VCCAUX_IO



VCC_HBM

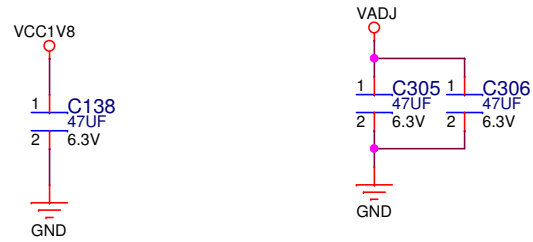
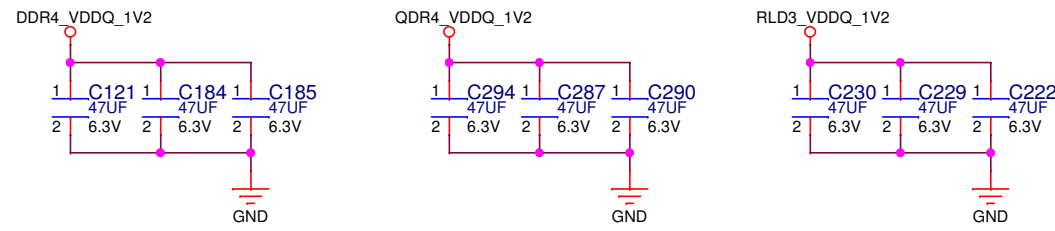


VCCAUX_HBM

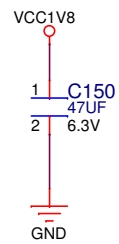


		PCB P/N : 1281016 ASSY P/N : 0432120 TEST P/N : TSS0201	
Title:		HW-U1-VCU128 020 FPGA Decoupling 1	
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VCCO (Banks 64 - 75)
(VCCO per bank 1x47uF)

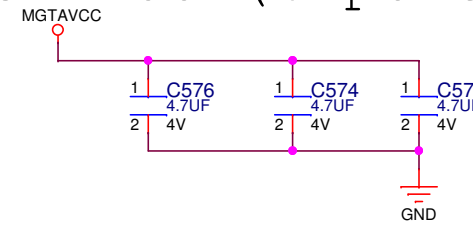


VCCAUX (Bank 0 Vcco)

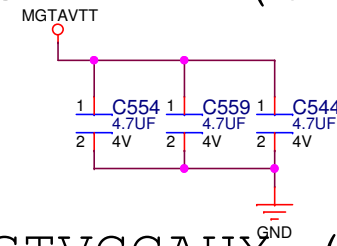


MGT decoupling from UG578 1x4.7uF per rail per power bank

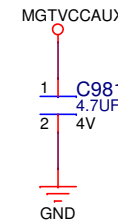
MGTAVCC (6 power banks)



MGTAVTT (6 power banks)



MGTVCCAUX (6 power banks)



		PCB P/N : 1281016 ASSY P/N : 0432120 TEST P/N : TSS0201	
Title: HW-U1-VCU128 021 FPGA Decoupling 2			
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BANK GND_2

AK48	GND_AK48
AK49	GND_AK49
AK50	GND_AK50
AK54	GND_AK54
AK7	GND_AK7
AL16	GND_AL16
AL19	GND_AL19
AL23	GND_AL23
AL27	GND_AL27
AL3	GND_AL3
AL33	GND_AL33
AL37	GND_AL37
AL4	GND_AL4
AL47	GND_AL47
AL51	GND_AL51
AL7	GND_AL7
AM1	GND_AM1
AM14	GND_AM14
AM18	GND_AM18
AM20	GND_AM20
AM24	GND_AM24
AM28	GND_AM28
AM32	GND_AM32
AM36	GND_AM36
AM39	GND_AM39
AM45	GND_AM45
AM49	GND_AM49
AM50	GND_AM50
AM54	GND_AM54
AM7	GND_AM7
AN16	GND_AN16
AN19	GND_AN19
AN23	GND_AN23
AN27	GND_AN27
AN3	GND_AN3
AN33	GND_AN33
AN37	GND_AN37
AN4	GND_AN4
AN47	GND_AN47
AN51	GND_AN51
AN7	GND_AN7
AP1	GND_AP1
AP14	GND_AP14
AP18	GND_AP18
AP20	GND_AP20
AP24	GND_AP24
AP28	GND_AP28
AP32	GND_AP32
AP36	GND_AP36
AP39	GND_AP39
AP45	GND_AP45
AP49	GND_AP49
AP50	GND_AP50
AP54	GND_AP54
AP7	GND_AP7
AR16	GND_AR16
AR19	GND_AR19
AR23	GND_AR23
AR27	GND_AR27
AR3	GND_AR3
AR33	GND_AR33
AR37	GND_AR37
AR4	GND_AR4
AR47	GND_AR47
AR50	GND_AR50
AR52	GND_AR52
AT1	GND_AT1
AT14	GND_AT14
AT18	GND_AT18
AT20	GND_AT20
AT24	GND_AT24
AT28	GND_AT28
AT32	GND_AT32
AT36	GND_AT36
AT39	GND_AT39
AT45	GND_AT45
AT49	GND_AT49
AT50	GND_AT50
AT54	GND_AT54
AT7	GND_AT7
AU16	GND_AU16
AU19	GND_AU19
AU23	GND_AU23
AU27	GND_AU27
AU3	GND_AU3
AU33	GND_AU33
AU37	GND_AU37
AU4	GND_AU4
AU47	GND_AU47
AU50	GND_AU50
AU52	GND_AU52
AV1	GND_AV1
AV14	GND_AV14
AV16	GND_AV16
AV2	GND_AV2
AV22	GND_AV22
AV26	GND_AV26
AV30	GND_AV30
AV34	GND_AV34
AV38	GND_AV38
AV40	GND_AV40
AV45	GND_AV45
AV49	GND_AV49
AV50	GND_AV50
AV54	GND_AV54
AV7	GND_AV7
AW13	GND_AW13
AW17	GND_AW17
AW21	GND_AW21
AW25	GND_AW25
AW29	GND_AW29
AW31	GND_AW31
AW35	GND_AW35
AW39	GND_AW39
AW41	GND_AW41
AW43	GND_AW43
AW48	GND_AW48
AW52	GND_AW52
AW8	GND_AW8
AY10	GND_AY10
AY16	GND_AY16
AY2	GND_AY2
AY22	GND_AY22
AY26	GND_AY26
AY30	GND_AY30
AY34	GND_AY34


U1-41 GND
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XCVU37PFSVH2892

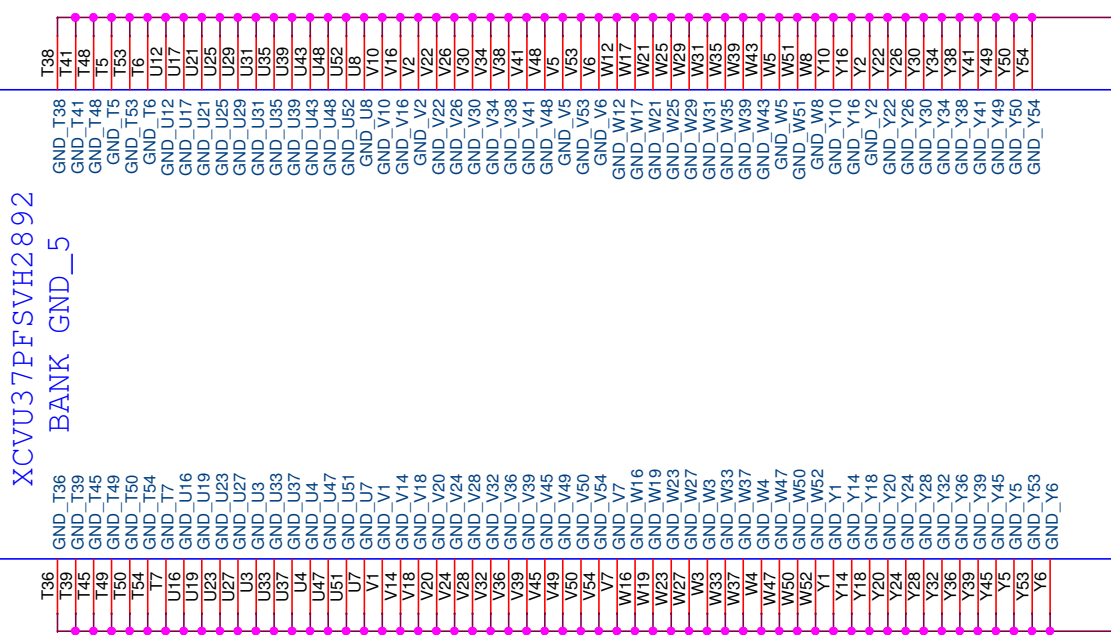
BANK GND_1

A12	GND_A12
A22	GND_A22
A32	GND_A32
A4	GND_A4
A47	GND_A47
A51	GND_A51
AA12	GND_AA12
AA21	GND_AA21
AA29	GND_AA29
AA31	GND_AA31
AA35	GND_AA35
AA43	GND_AA43
AA5	GND_AA5
AA51	GND_AA51
AA8	GND_AA8
AB10	GND_AB10
AB16	GND_AB16
AB2	GND_AB2
AB22	GND_AB22
AB26	GND_AB26
AB32	GND_AB32
AB36	GND_AB36
AB45	GND_AB45
AB49	GND_AB49
AB54	GND_AB54
AB7	GND_AB7
AB7	GND_AB7
AC16	GND_AC16
AC19	GND_AC19
AC23	GND_AC23
AC29	GND_AC29
AC31	GND_AC31
AC35	GND_AC35
AC43	GND_AC43
AC48	GND_AC48
AC52	GND_AC52
AC8	GND_AC8
AD10	GND_AD10
AD16	GND_AD16
AD2	GND_AD2
AD22	GND_AD22
AD26	GND_AD26
AD32	GND_AD32
AD36	GND_AD36
AD39	GND_AD39
AD45	GND_AD45
AD49	GND_AD49
AD50	GND_AD50
AD54	GND_AD54
AD7	GND_AD7
AE16	GND_AE16
AE19	GND_AE19
AE23	GND_AE23
AE29	GND_AE29
AE31	GND_AE31
AE35	GND_AE35
AE39	GND_AE39
AE43	GND_AE43
AE48	GND_AE48
AE52	GND_AE52
AEB	GND_AEB
AF10	GND_AF10
AF16	GND_AF16
AF2	GND_AF2
AF22	GND_AF22
AF26	GND_AF26
AF30	GND_AF30
AF34	GND_AF34
AF38	GND_AF38
AF41	GND_AF41
AF48	GND_AF48
AF5	GND_AF5
AF53	GND_AF53
AF6	GND_AF6
AG12	GND_AG12
AG17	GND_AG17
AG21	GND_AG21
AG25	GND_AG25
AG29	GND_AG29
AG31	GND_AG31
AG33	GND_AG33
AG39	GND_AG39
AG47	GND_AG47
AG5	GND_AG5
AG51	GND_AG51
AG8	GND_AG8
AH10	GND_AH10
AH16	GND_AH16
AH2	GND_AH2
AH22	GND_AH22
AH26	GND_AH26
AH30	GND_AH30
AH34	GND_AH34
AH38	GND_AH38
AH41	GND_AH41
AH48	GND_AH48
AH5	GND_AH5
AH53	GND_AH53
AH6	GND_AH6
AJ12	GND_AJ12
AJ17	GND_AJ17
AJ21	GND_AJ21
AJ25	GND_AJ25
AJ29	GND_AJ29
AJ31	GND_AJ31
AJ35	GND_AJ35
AJ39	GND_AJ39
AJ43	GND_AJ43
AJ5	GND_AJ5
AJ51	GND_AJ51
AJ8	GND_AJ8
AK10	GND_AK10
AK16	GND_AK16
AK2	GND_AK2
AK22	GND_AK22
AK26	GND_AK26
AK30	GND_AK30
AK34	GND_AK34
AK38	GND_AK38
AK41	GND_AK41

U1-40 GND
FPGA-XCVU37P-H2892

		PCB P/N : 1281016 ASSY P/N : 0432120 TEST P/N : TSS0201	
Title:		HW-U1-VCU128 022 FPGA GND 1	
Size B	Date Modified: Wednesday, October 10, 2018	Document Number: 0381852	Ver 1.0
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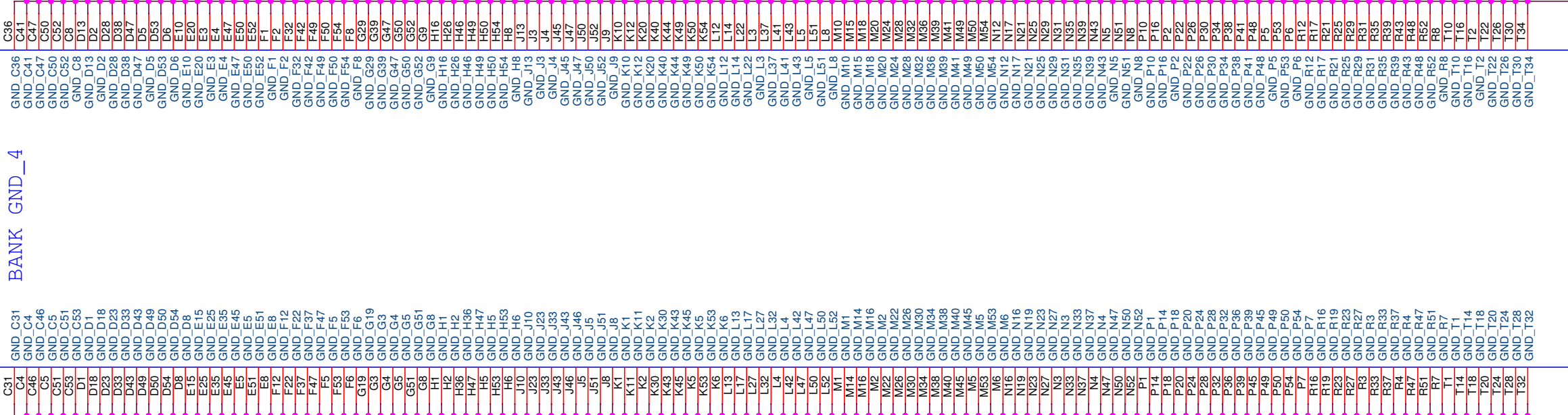
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BANK GND_5



U1-44
FPGA-XCVU37P-H2892

GND

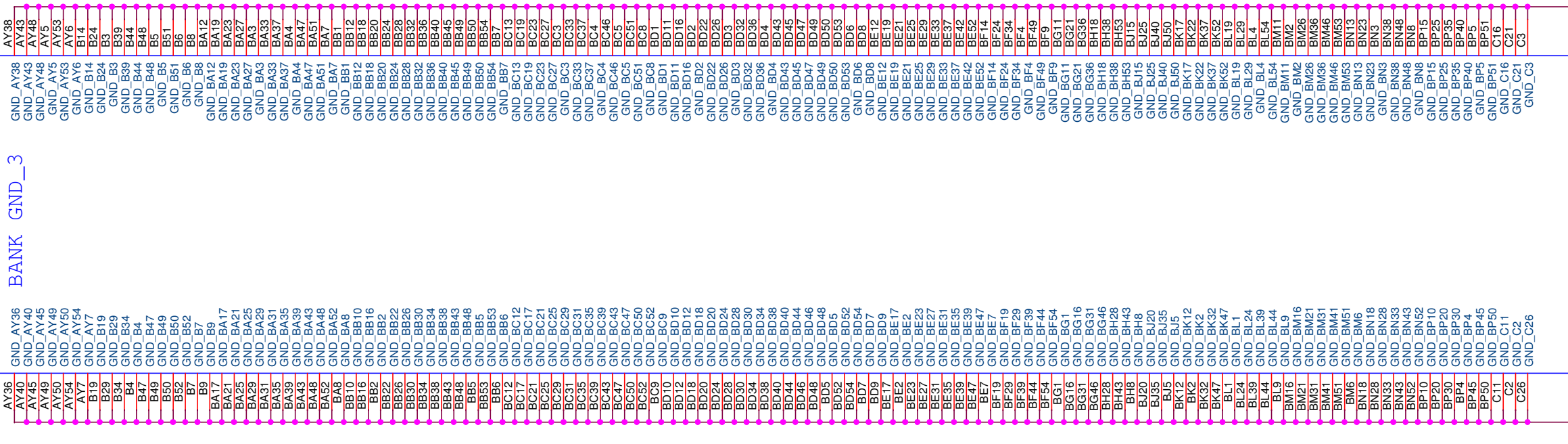
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BANK GND_4



U1-43
FPGA-XCVU37P-H2892

GND

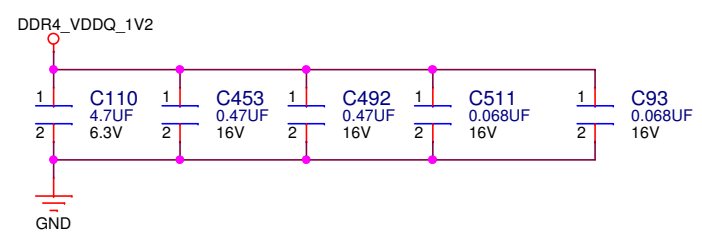
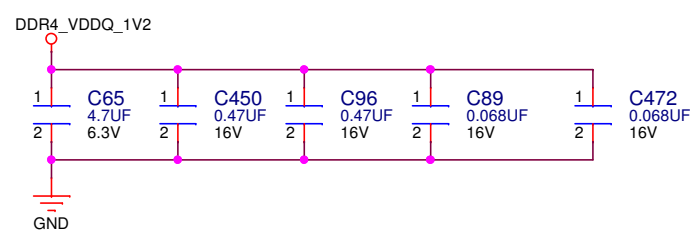
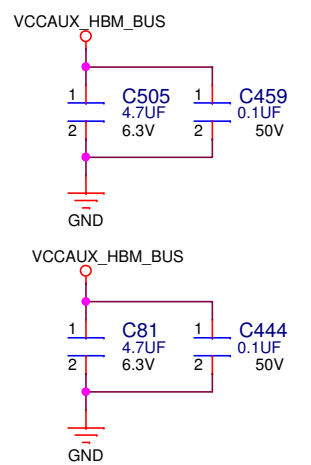
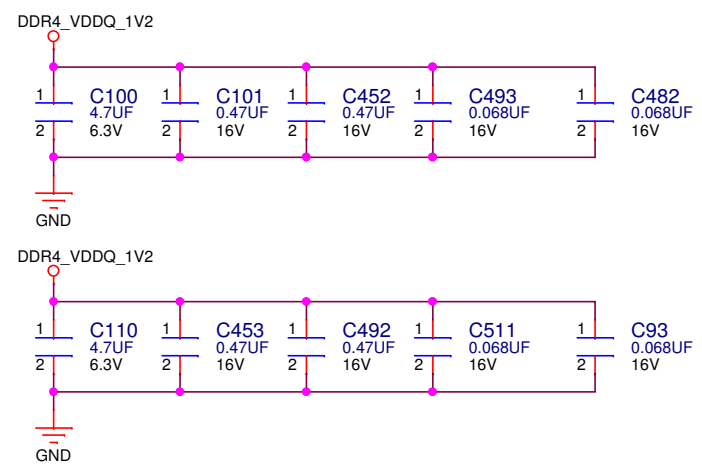
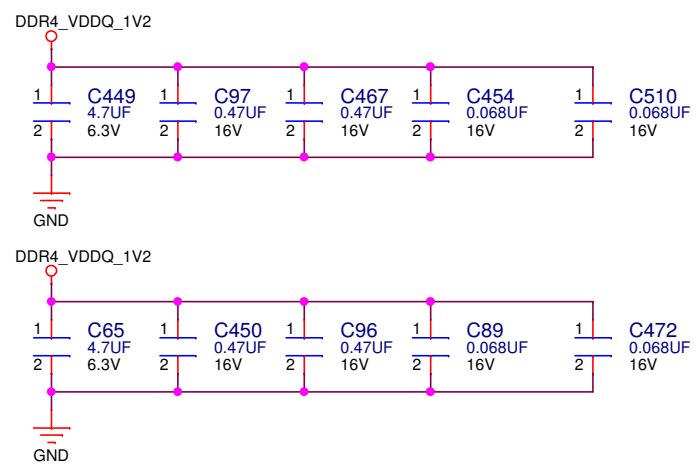
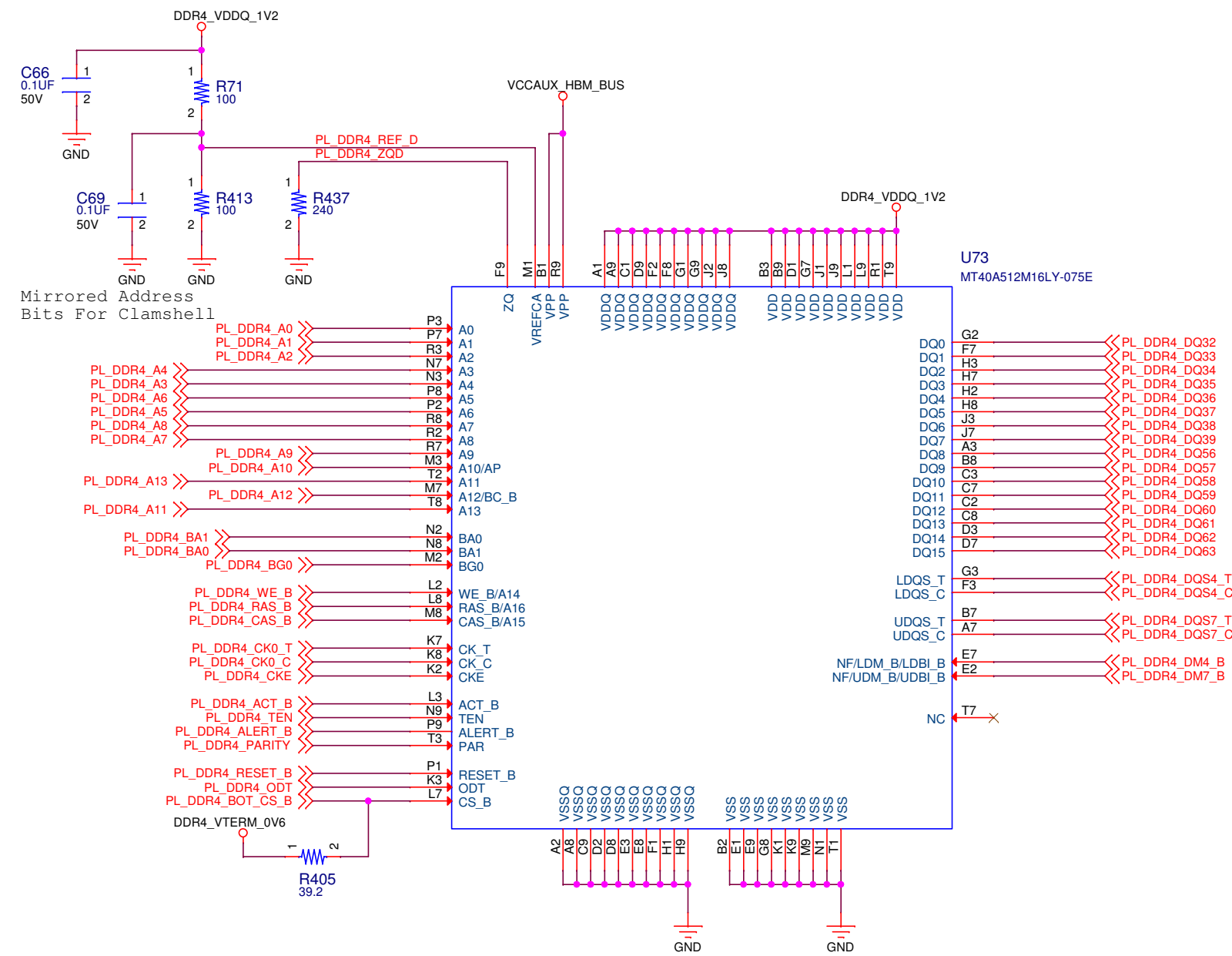
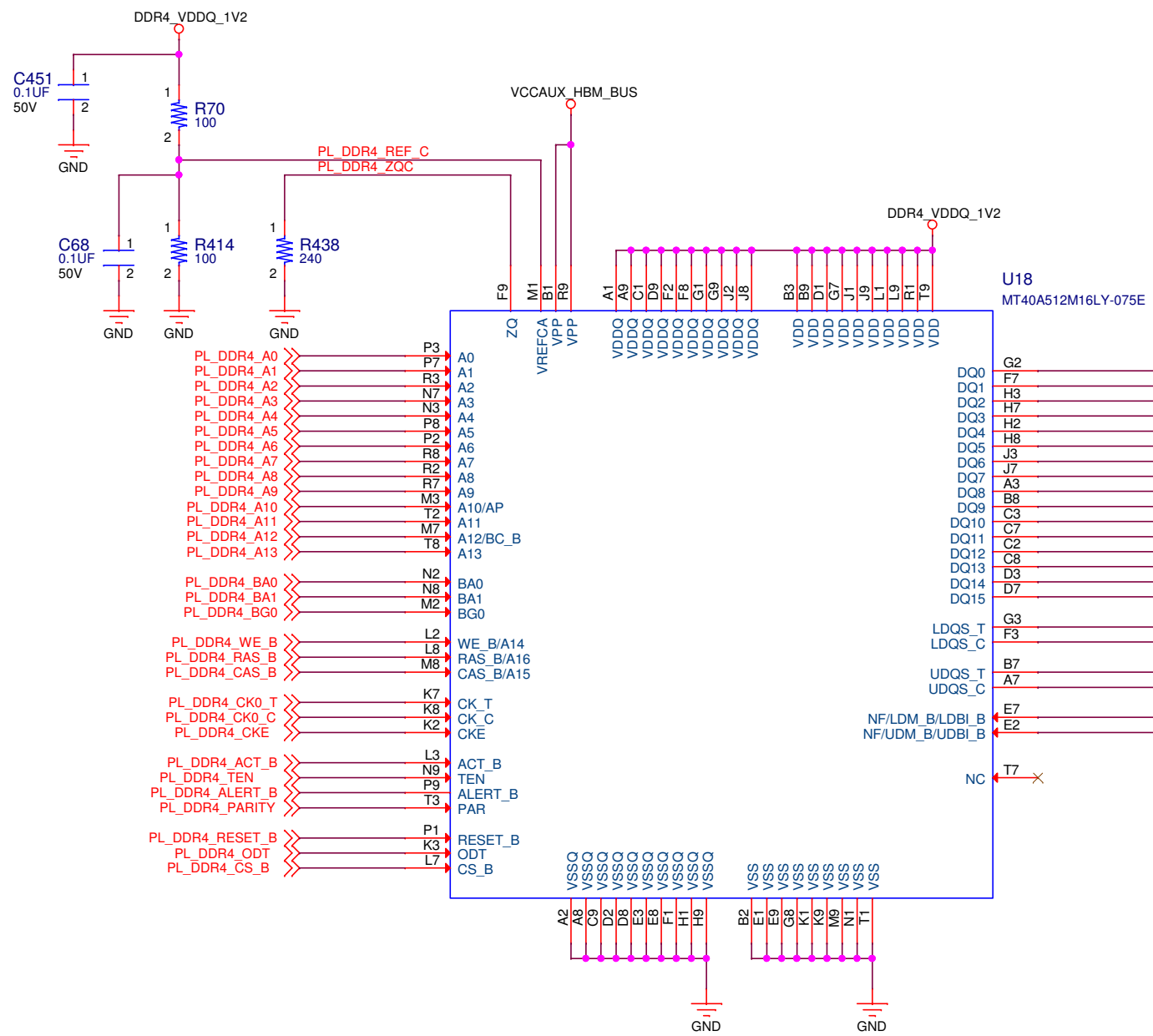
XCVU37PFSVH2892
BANK GND_3



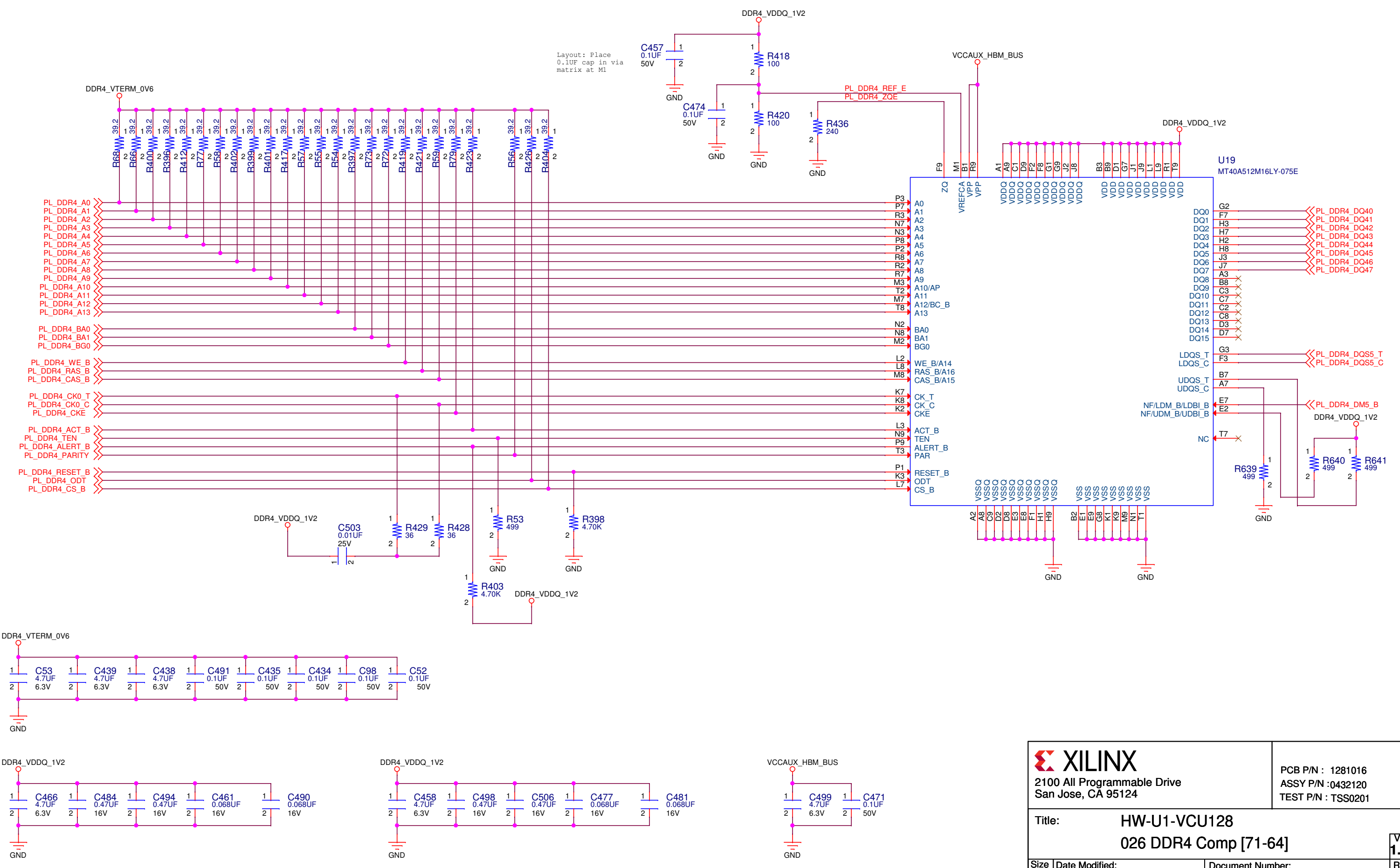
U1-42
FPGA-XCVU37P-H2892

GND

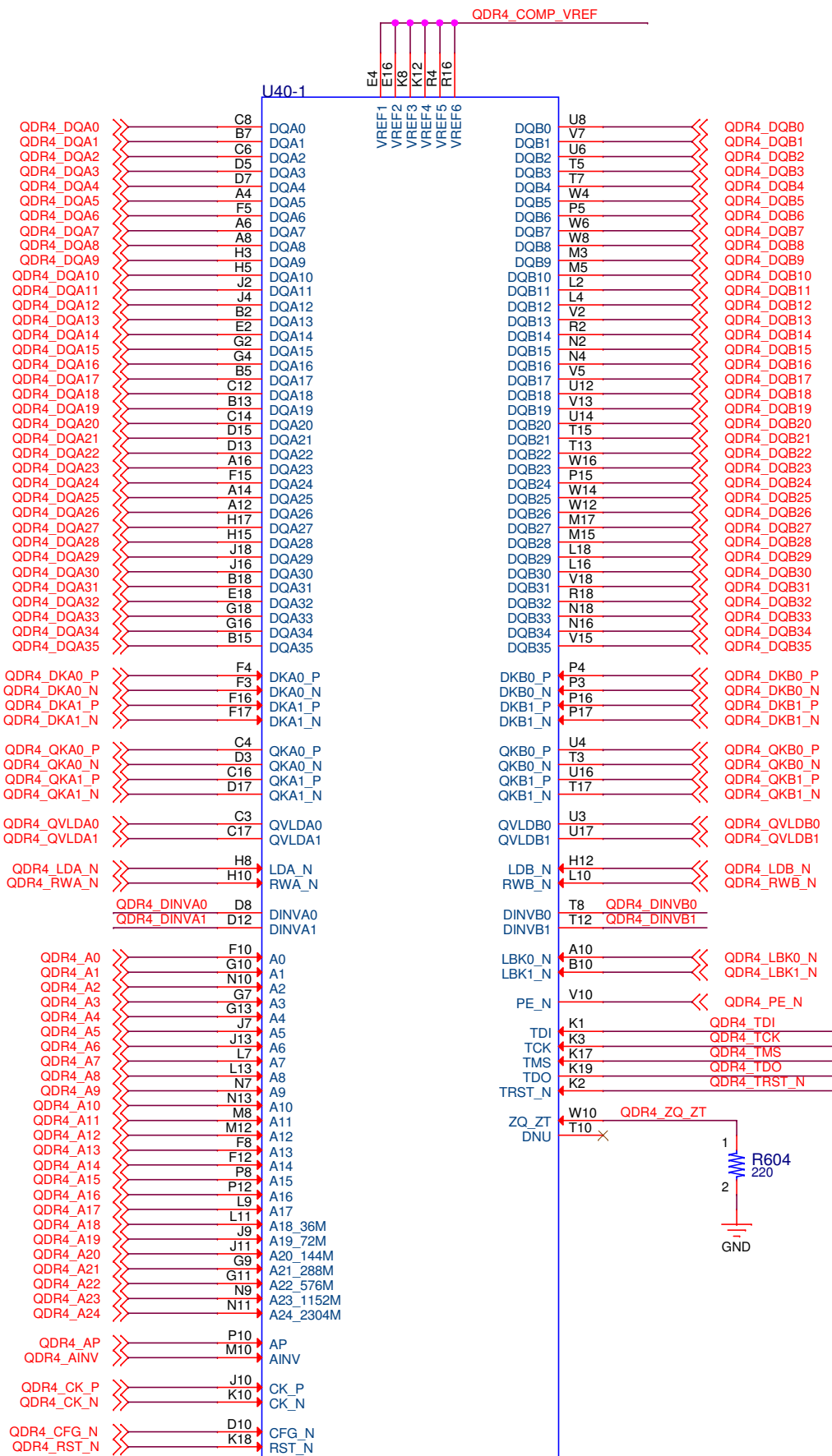
		PCB P/N : 1281016 ASSY P/N : 0432120 TEST P/N : TSS0201	
Title:		HW-U1-VCU128 023 FPGA GND 2	
Size B	Date Modified: Wednesday, October 10, 2018	Document Number: 0381852	Ver 1.0
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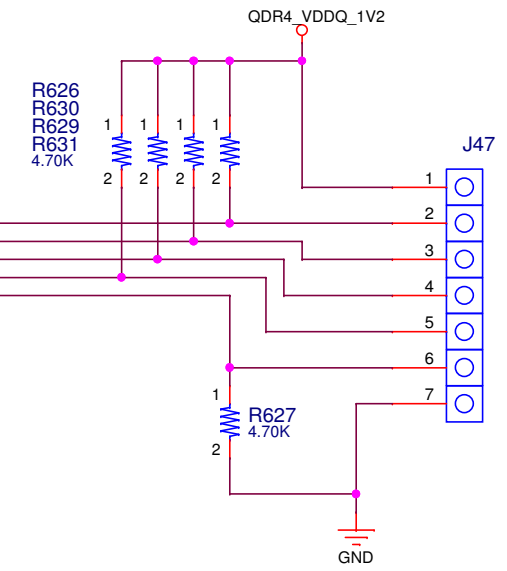
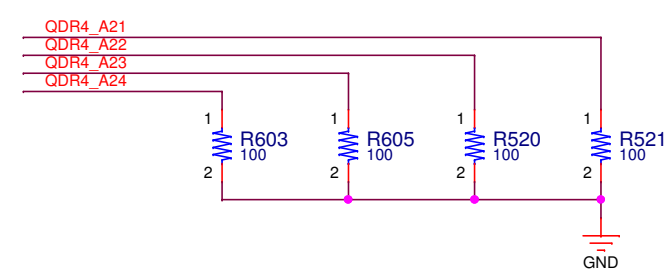
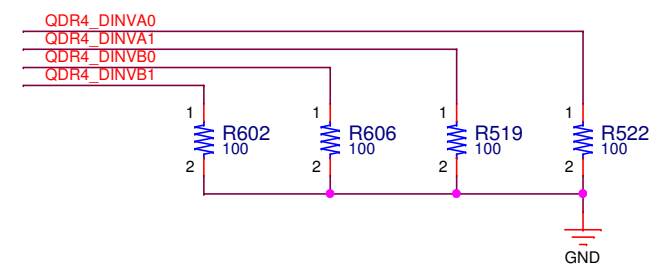
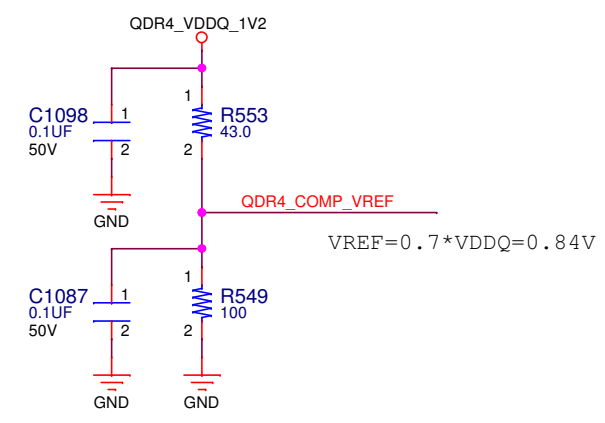
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Title: HW-U1-VCU128 025 DDR4 Comp [47-32], [63-48]			
Size B	Date Modified: Wednesday, October 10, 2018	Document Number: 0381852	Ver 1.0 Rev 01
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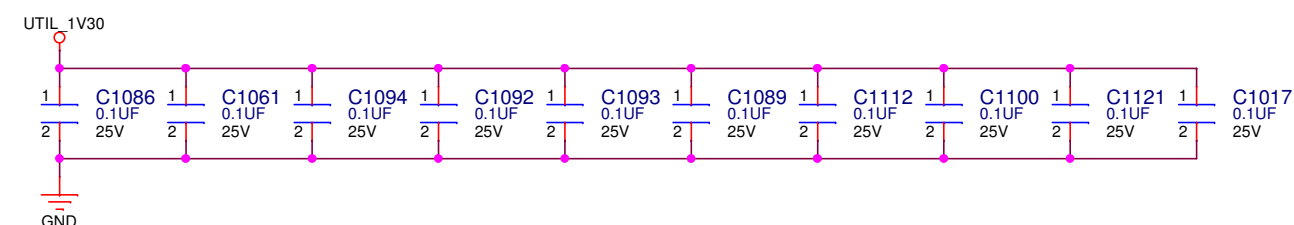
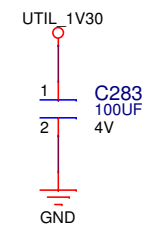
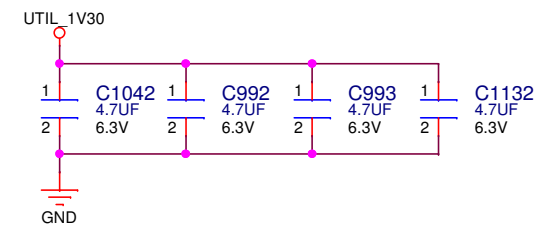
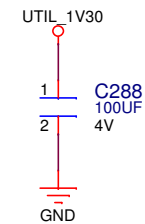
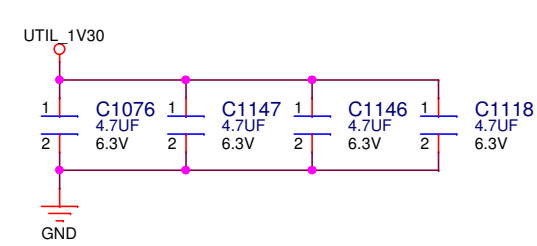
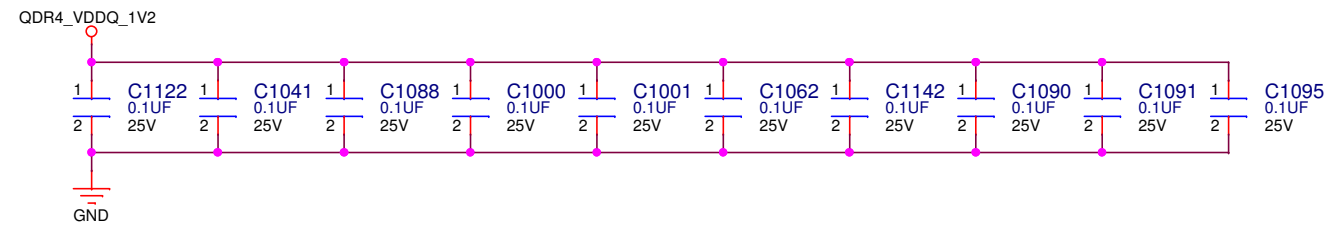
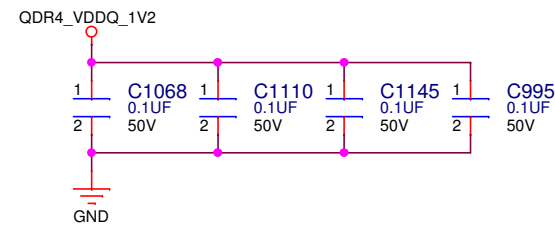
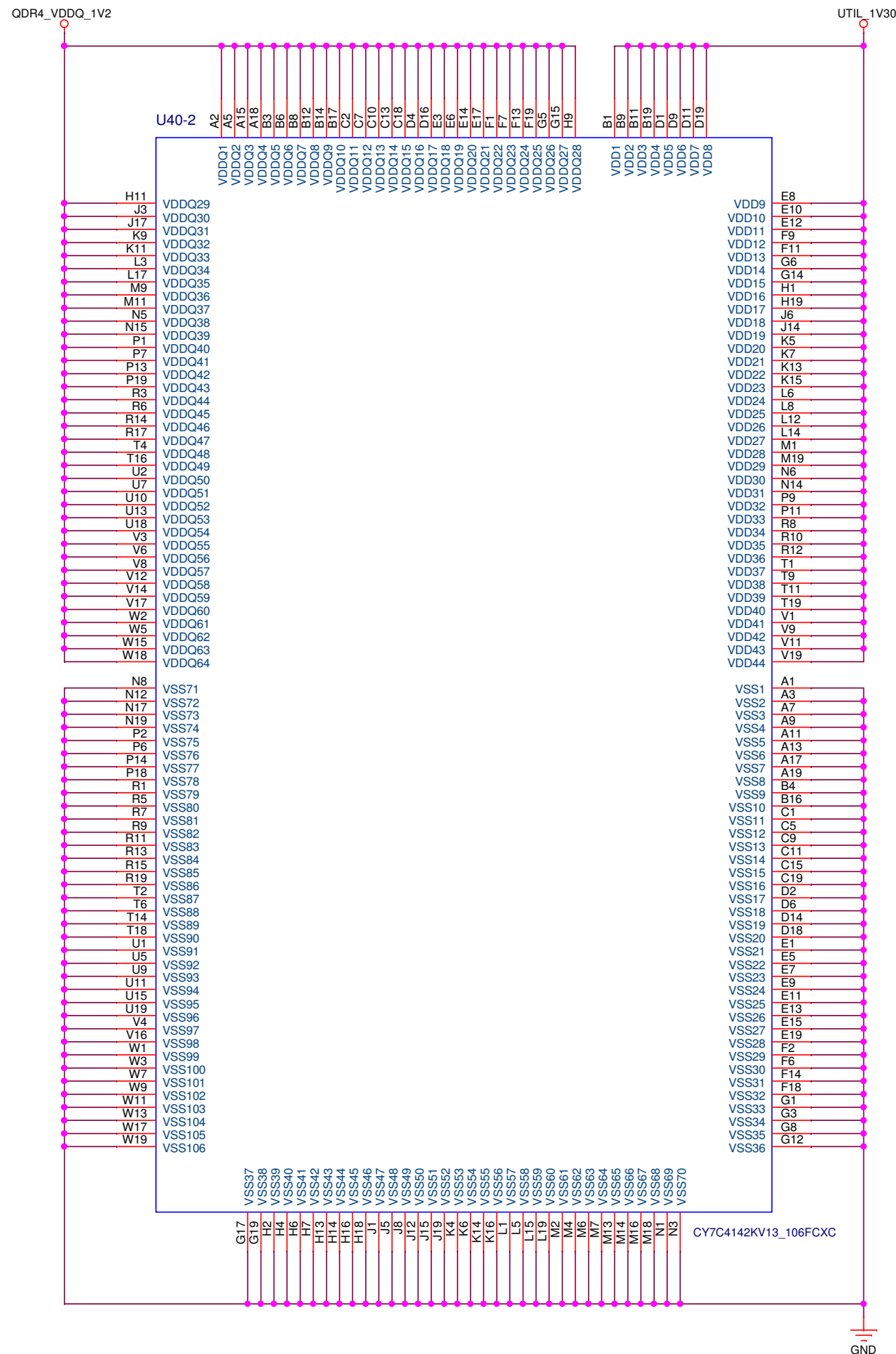
		PCB P/N : 1281016 ASSY P/N : 0432120 TEST P/N : TSS0201	
Title: HW-U1-VCU128 026 DDR4 Comp [71-64]			
Size B	Date Modified: Wednesday, October 10, 2018	Document Number: 0381852	Ver 1.0 Rev 01
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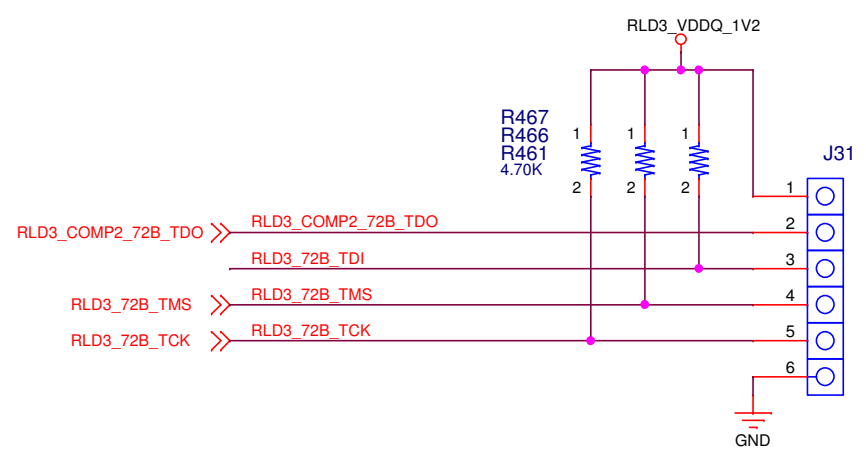
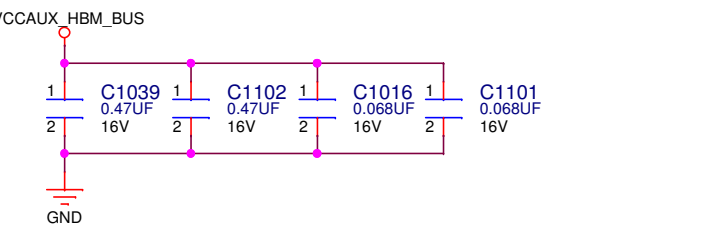
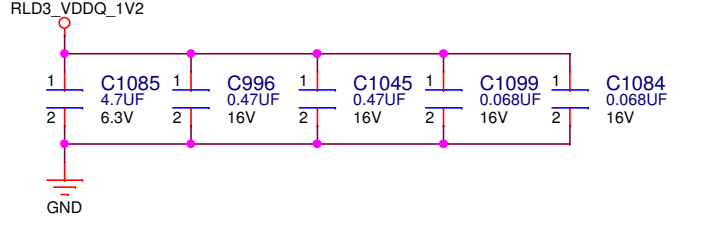
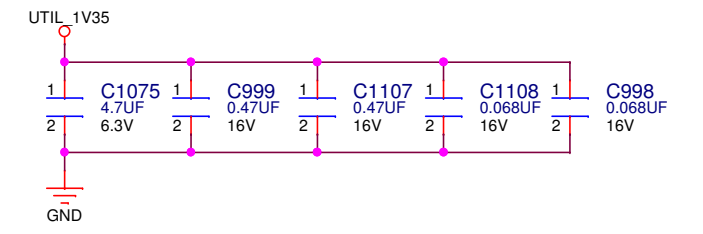
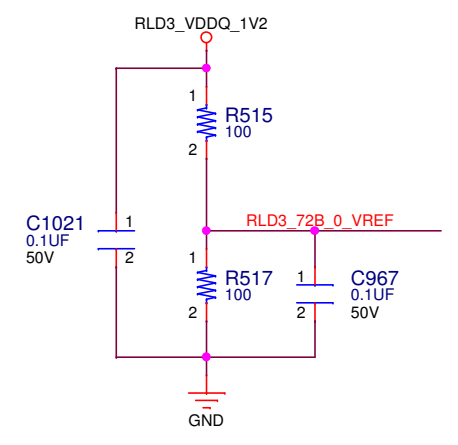
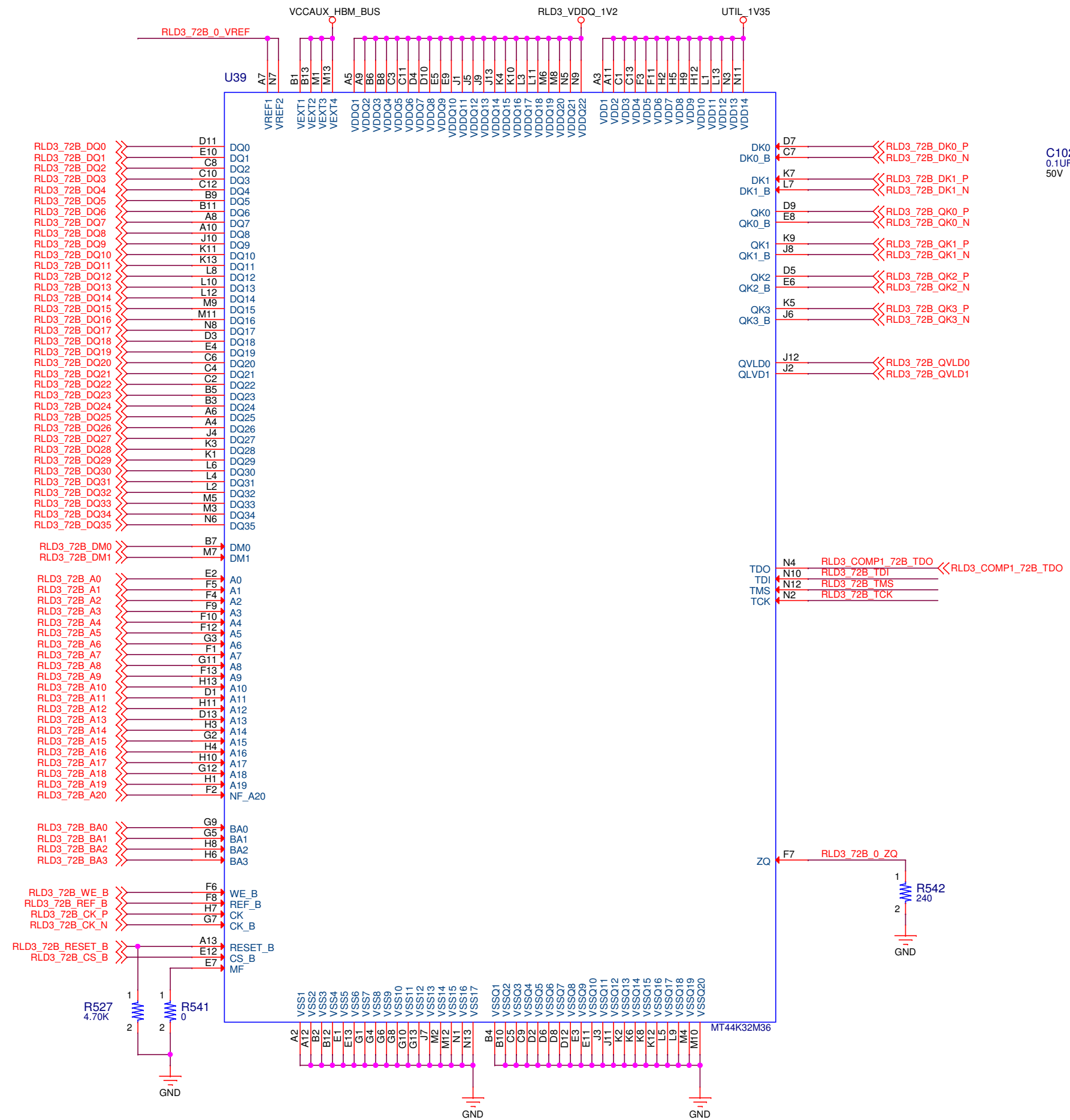
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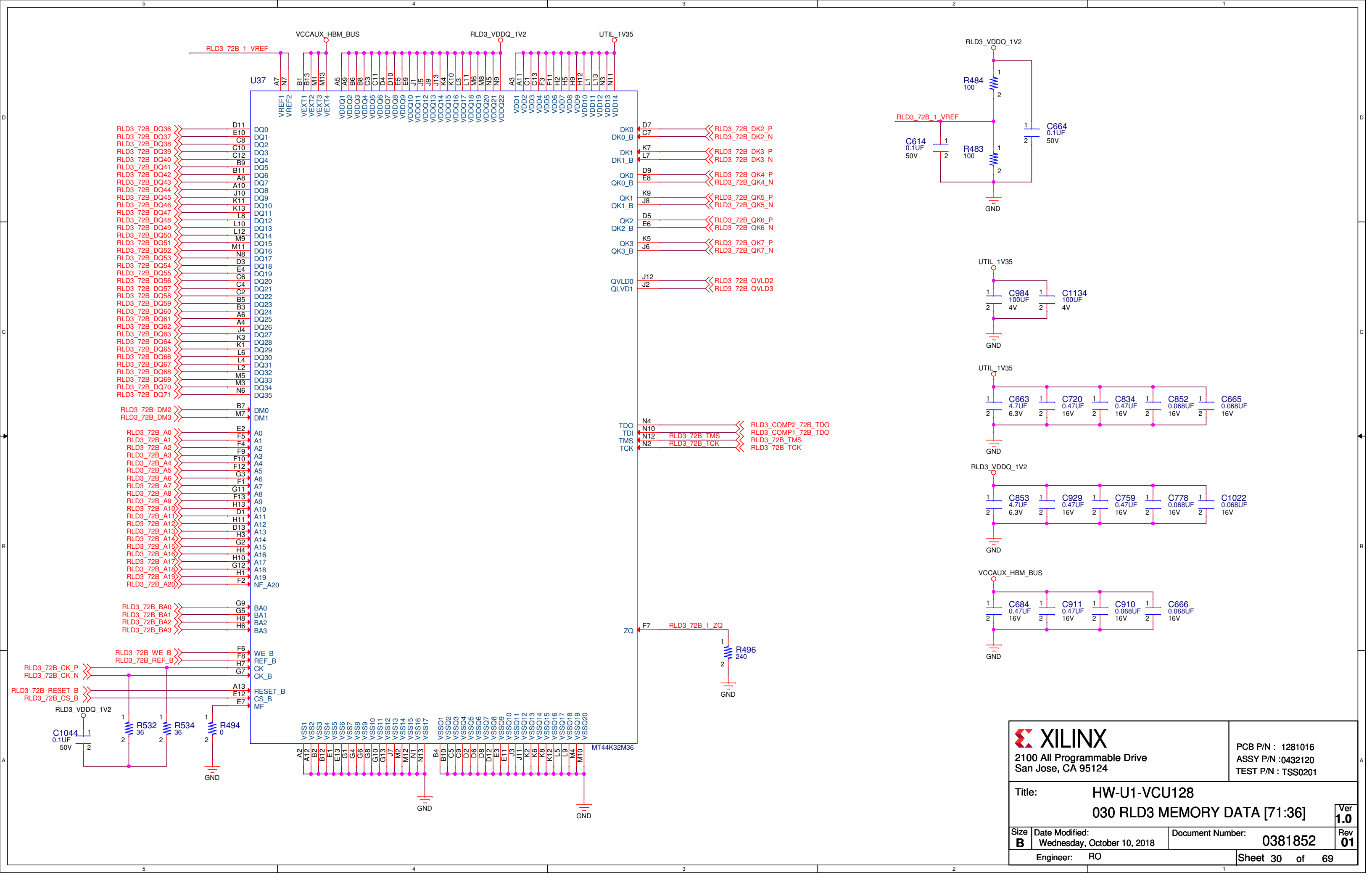
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Title:		HW-U1-VCU128 027 QDR4 Comp Data	
Size B	Date Modified: Wednesday, October 10, 2018	Document Number: 0381852	Ver 1.0 Rev 01
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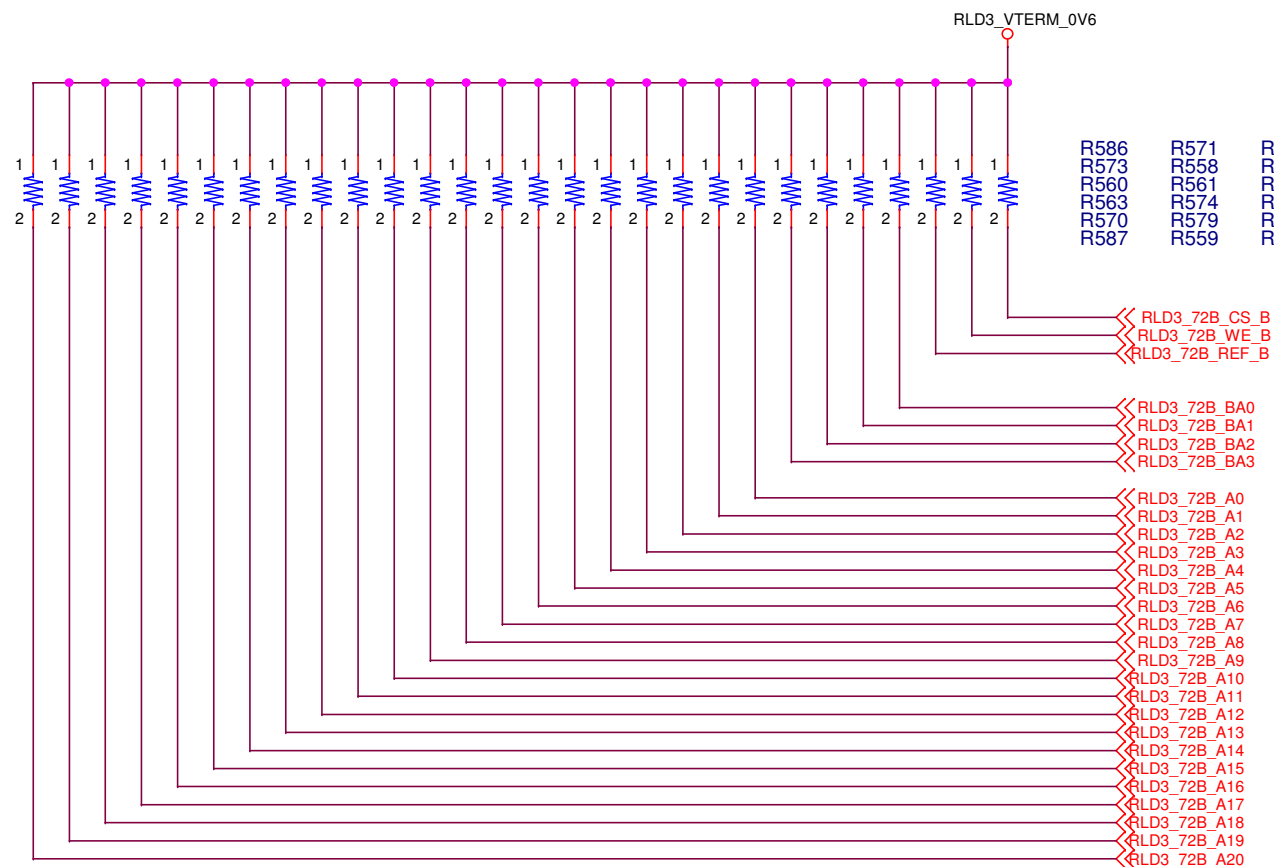
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Title: HW-U1-VCU128 028 QDR4 Comp Power			
Size B	Date Modified: Wednesday, October 10, 2018	Document Number: 0381852	Ver 1.0 Rev 01
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		PCB P/N : 1281016 ASSY P/N : 0432120 TEST P/N : TSS0201	
Title: HW-U1-VCU128 029 RLD3 MEMORY DATA [35:0]			
Size	Date Modified:	Document Number:	Ver
B	Wednesday, October 10, 2018	0381852	1.0
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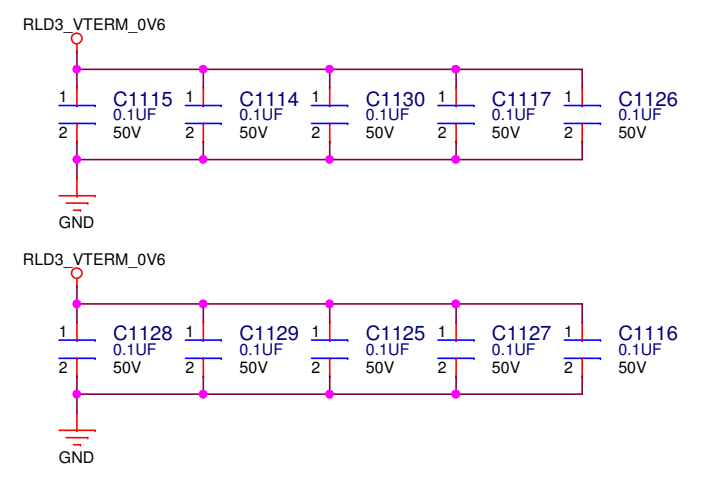
		PCB P/N : 1281016 ASSY P/N : 0432120 TEST P/N : TSS0201	
Title: HW-U1-VCU128 030 RLD3 MEMORY DATA [71:36]			
Size B	Date Modified: Wednesday, October 10, 2018	Document Number: 0381852	Ver 1.0 Rev 01
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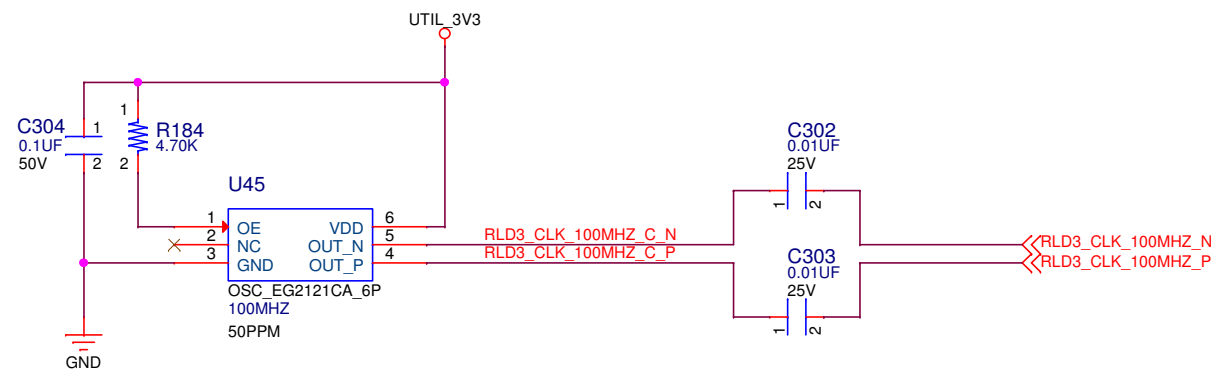
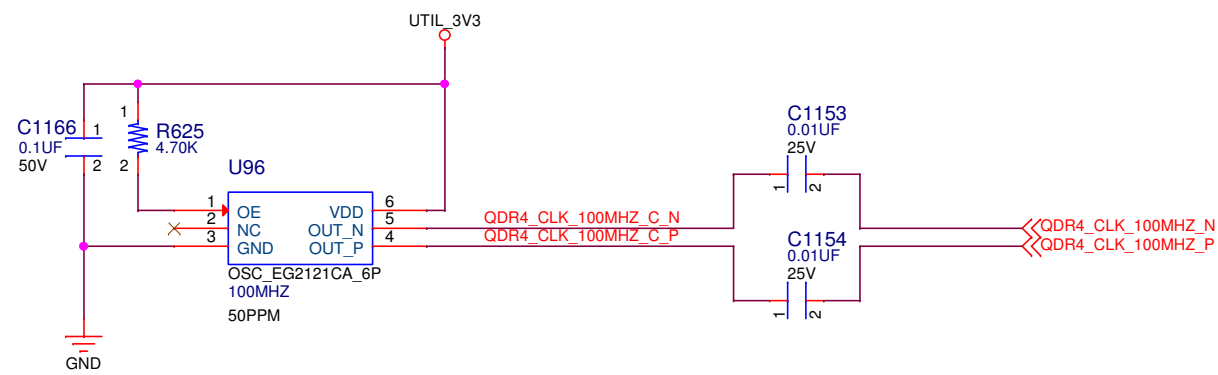
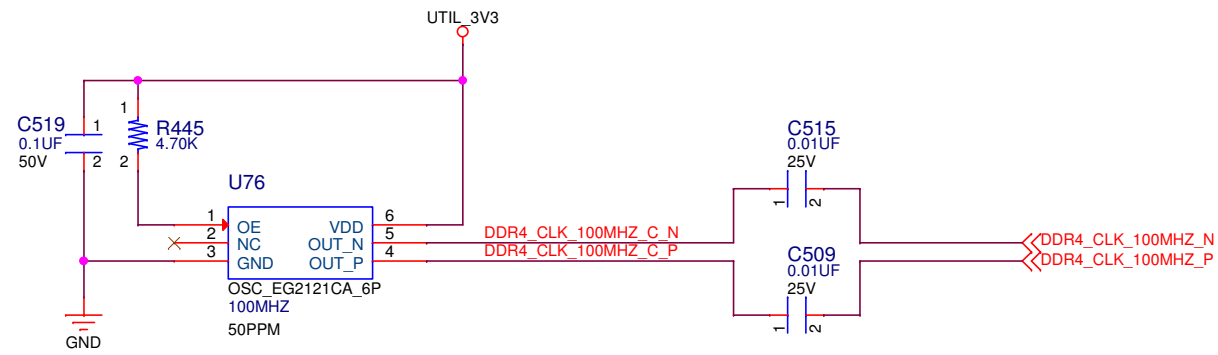
- R586
- R573
- R560
- R563
- R570
- R587
- R571
- R558
- R561
- R574
- R579
- R559
- R562
- R588
- R162
- R580
- R582
- R583
- R569
- R568
- R572
- R584
- R566
- R565
- R567
- R581
- 39.2

40 OHM TERMINATIONS
 PLACE TERM RESISTORS IN
 "FLYBY" CONFIGURATION
 AFTER LAST COMPONENT

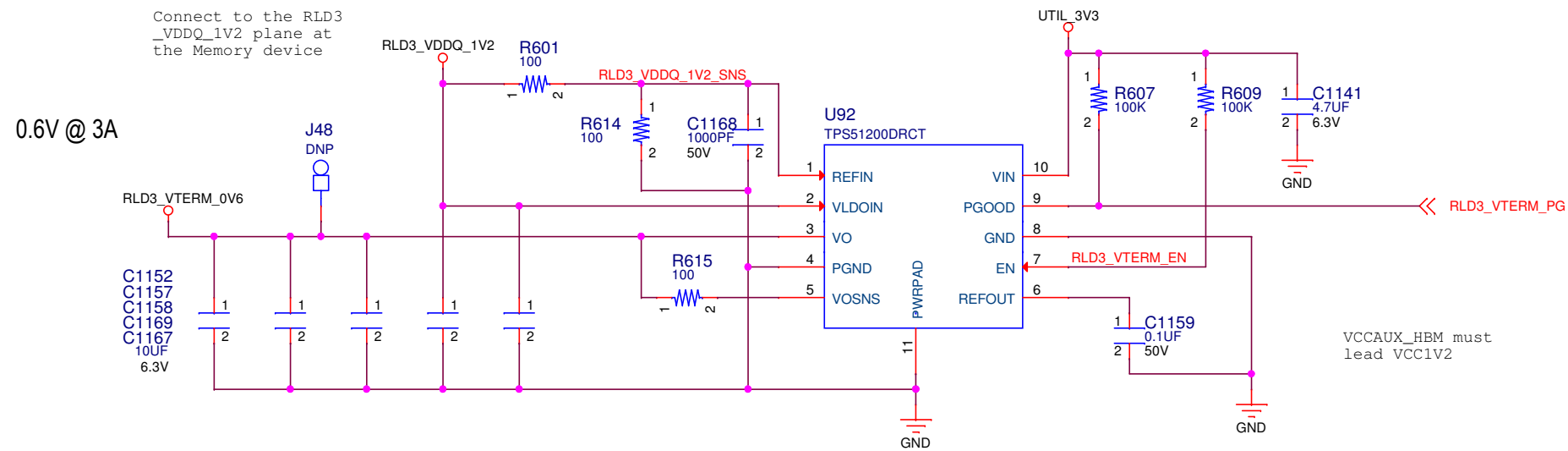
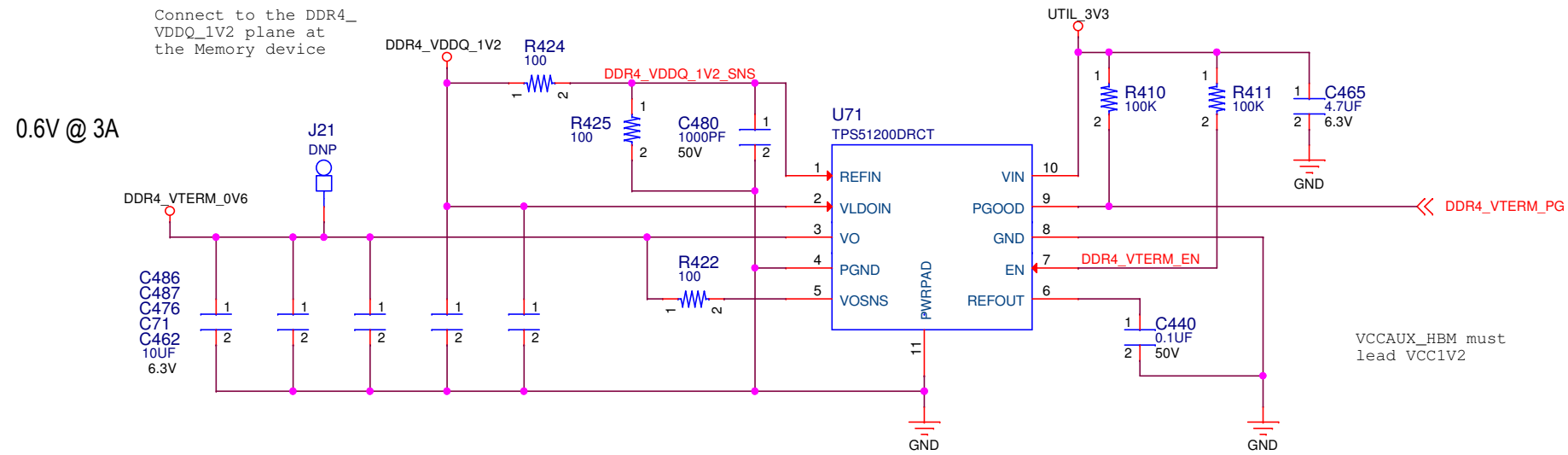
RLD3 C3 72-BIT RTERM DECOUPLING



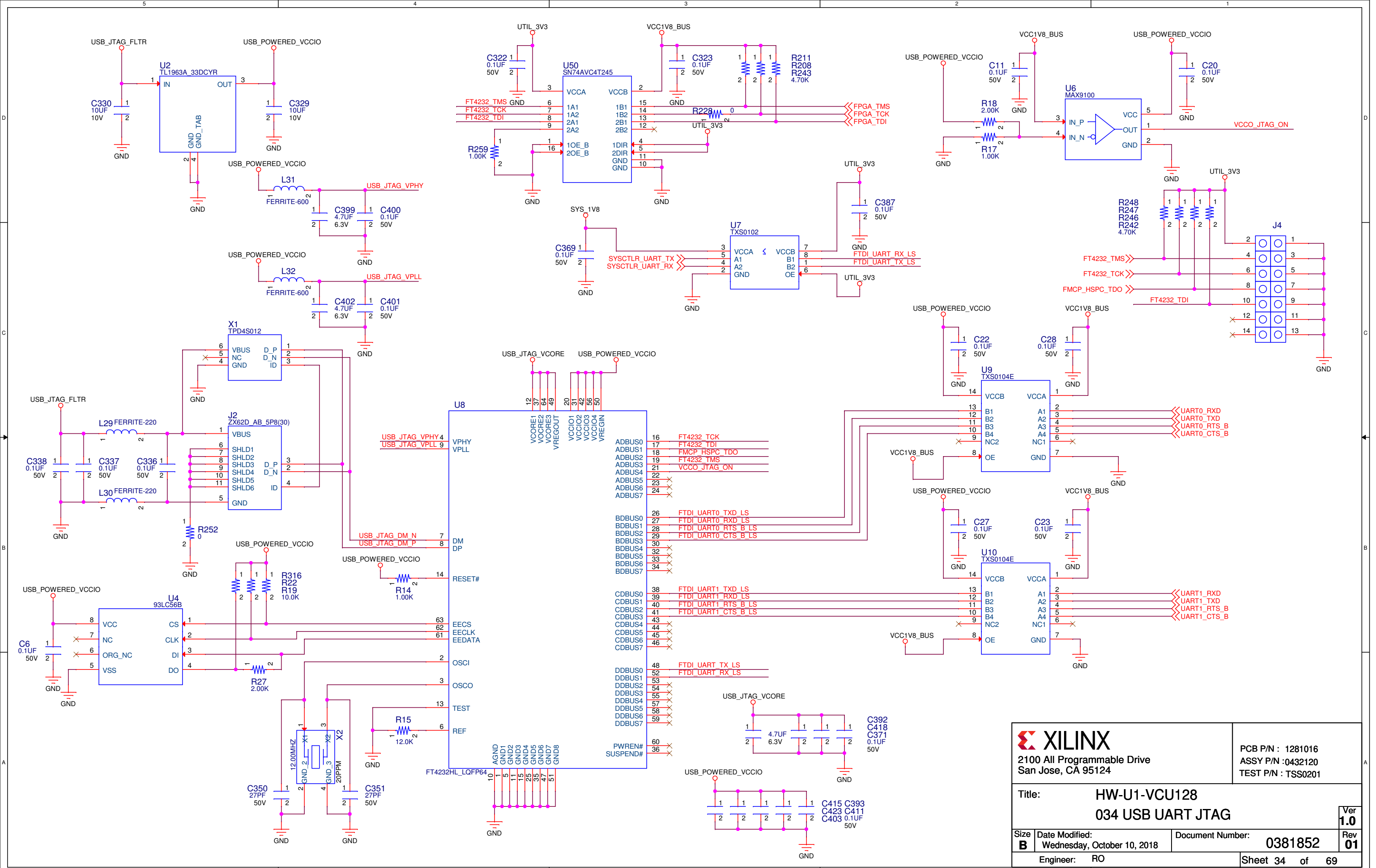
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Title:		HW-U1-VCU128 031 RLD3 MEMORY TERMINATION	
Size B	Date Modified: Wednesday, October 10, 2018	Document Number: 0381852	Ver 1.0 Rev 01
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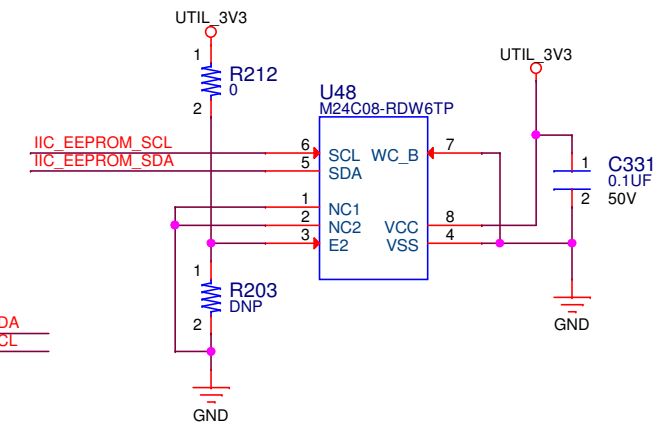
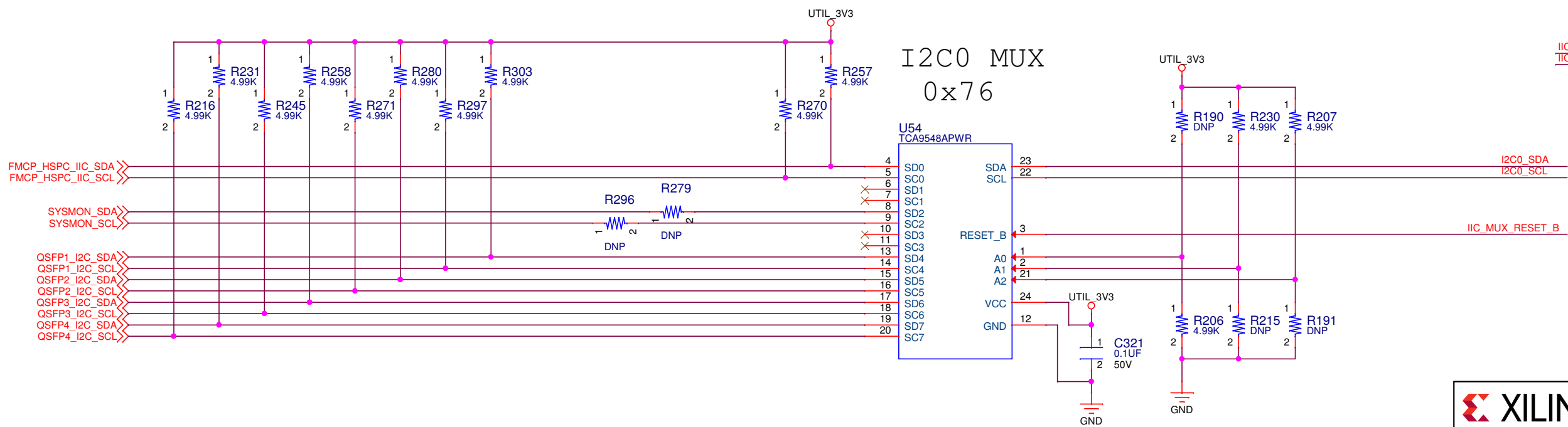
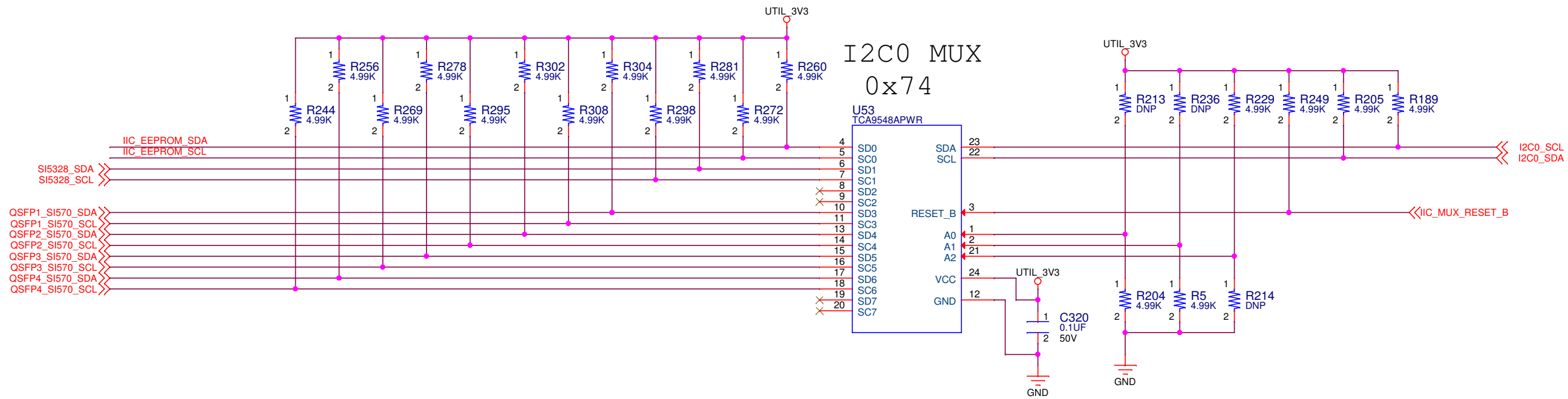
		PCB P/N : 1281016 ASSY P/N : 0432120 TEST P/N : TSS0201	
Title: HW-U1-VCU128 032 MEMORY CLOCKS			
Size B	Date Modified: Wednesday, October 10, 2018	Document Number: 0381852	Ver 1.0 Rev 01
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		PCB P/N : 1281016 ASSY P/N : 0432120 TEST P/N : TSS0201	
Title: HW-U1-VCU128 033 MEMORY VTT Regulators			
Size	Date Modified:	Document Number:	Ver
B	Wednesday, October 10, 2018	0381852	1.0
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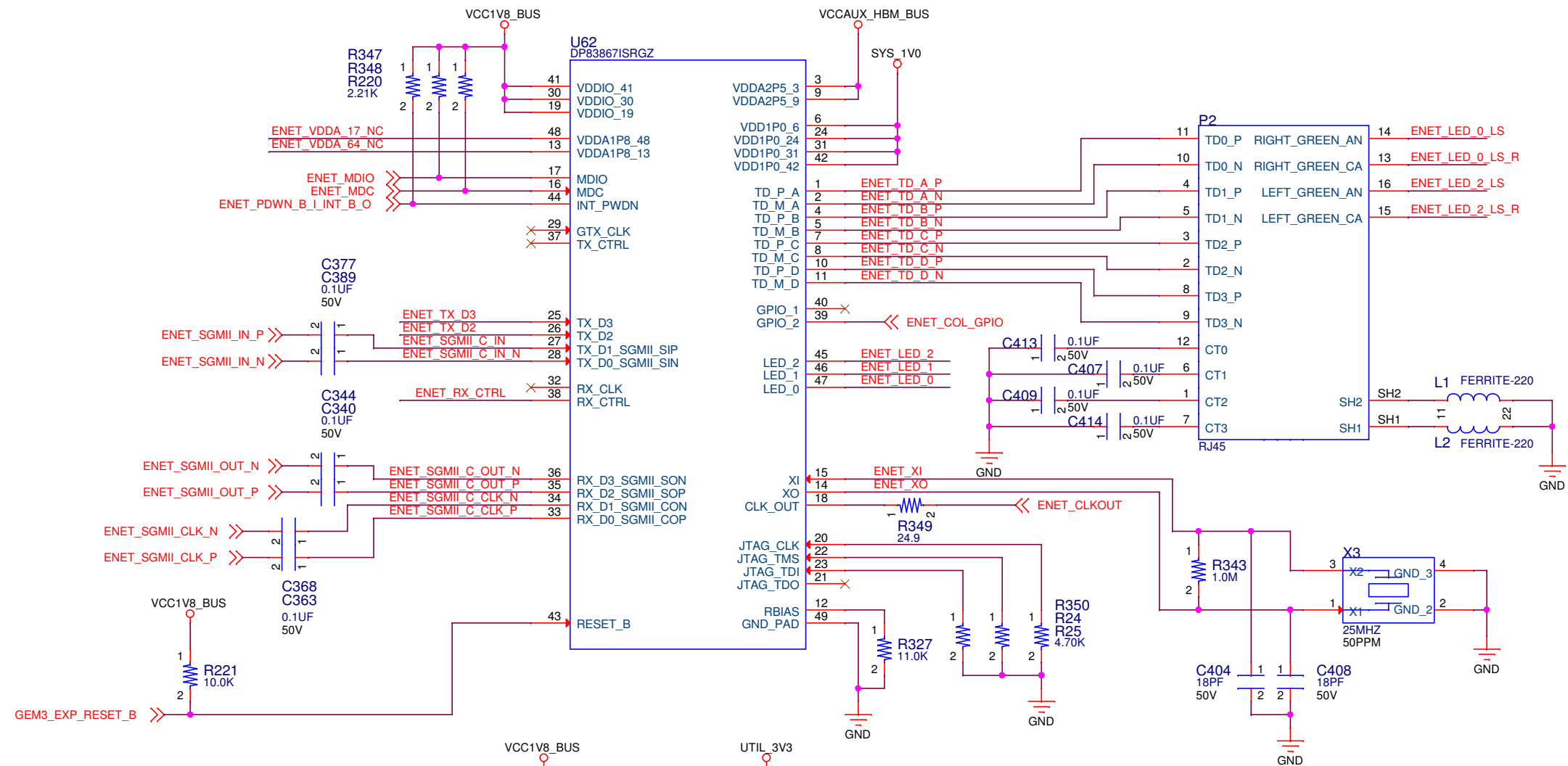
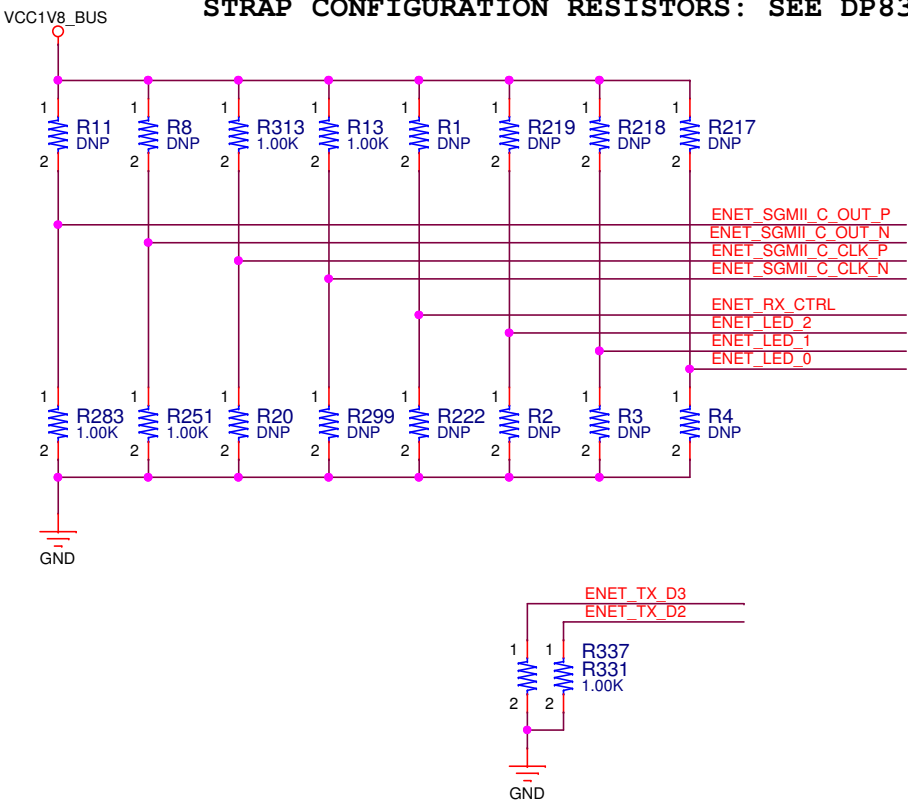


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Title:		HW-U1-VCU128 034 USB UART JTAG	
Size B	Date Modified: Wednesday, October 10, 2018	Document Number: 0381852	Ver 1.0 Rev 01
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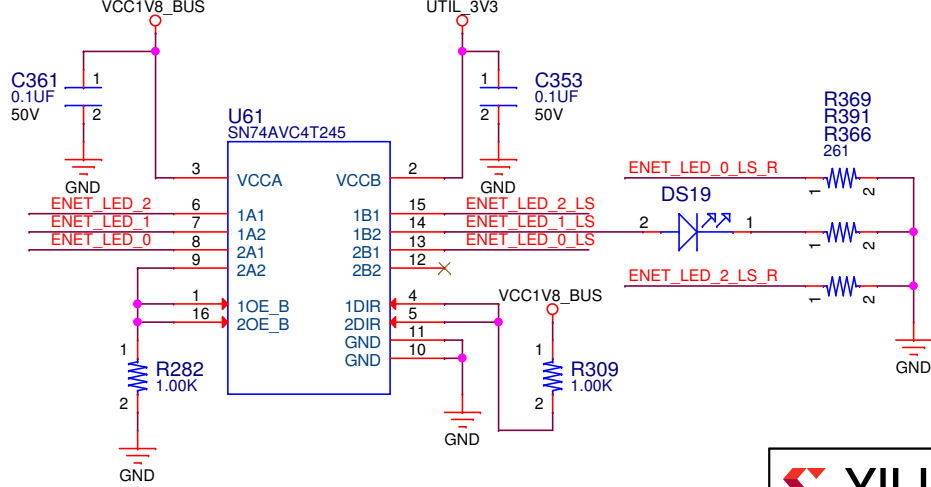
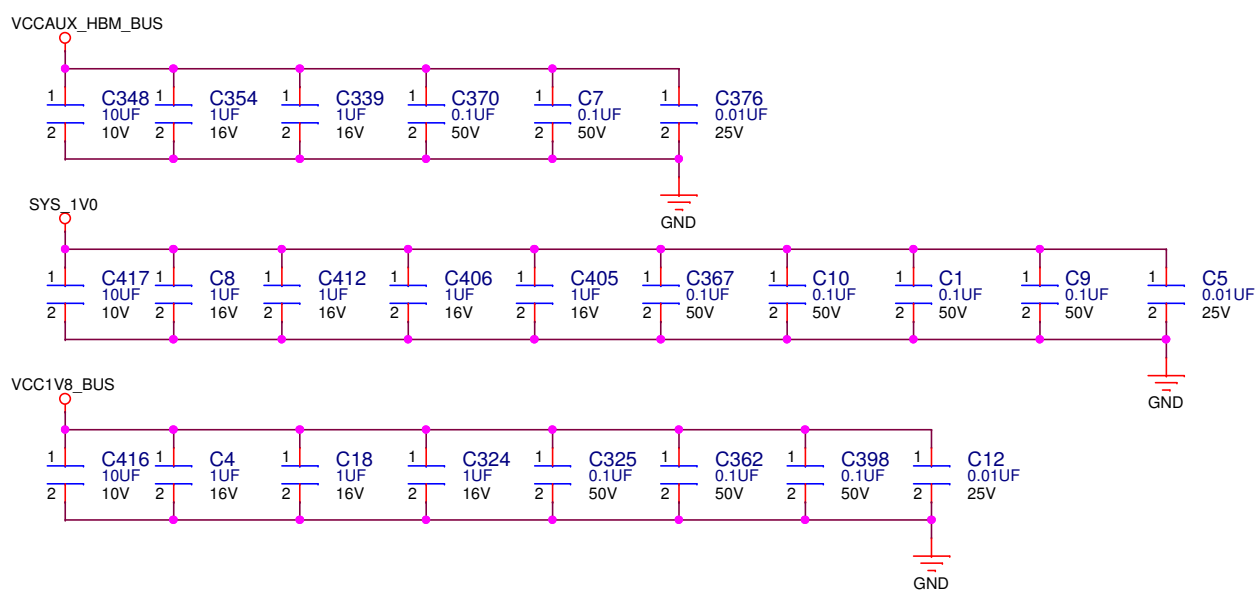


		PCB P/N : 1281016 ASSY P/N : 0432120 TEST P/N : TSS0201	
Title:		HW-U1-VCU128 036 I2C0 MUX 0x74 AND 0x76	
Size B	Date Modified: Wednesday, October 10, 2018	Document Number: 0381852	Ver 1.0 Rev 01
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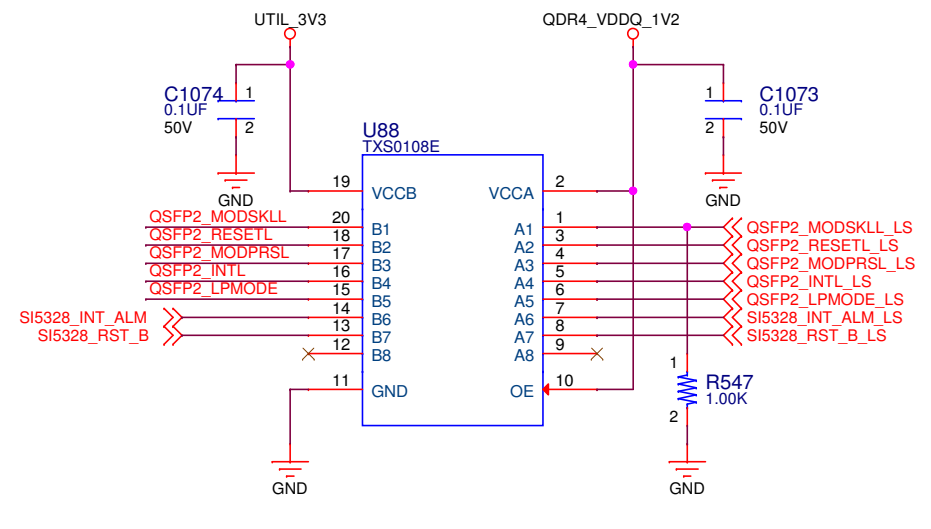
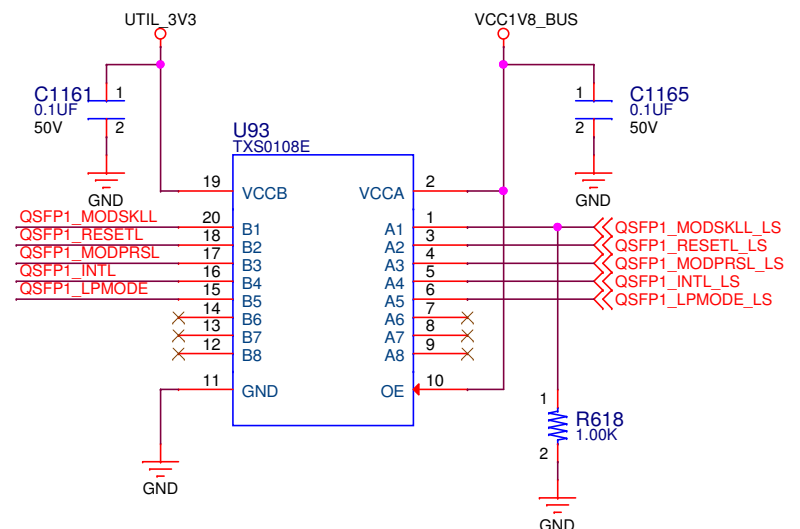
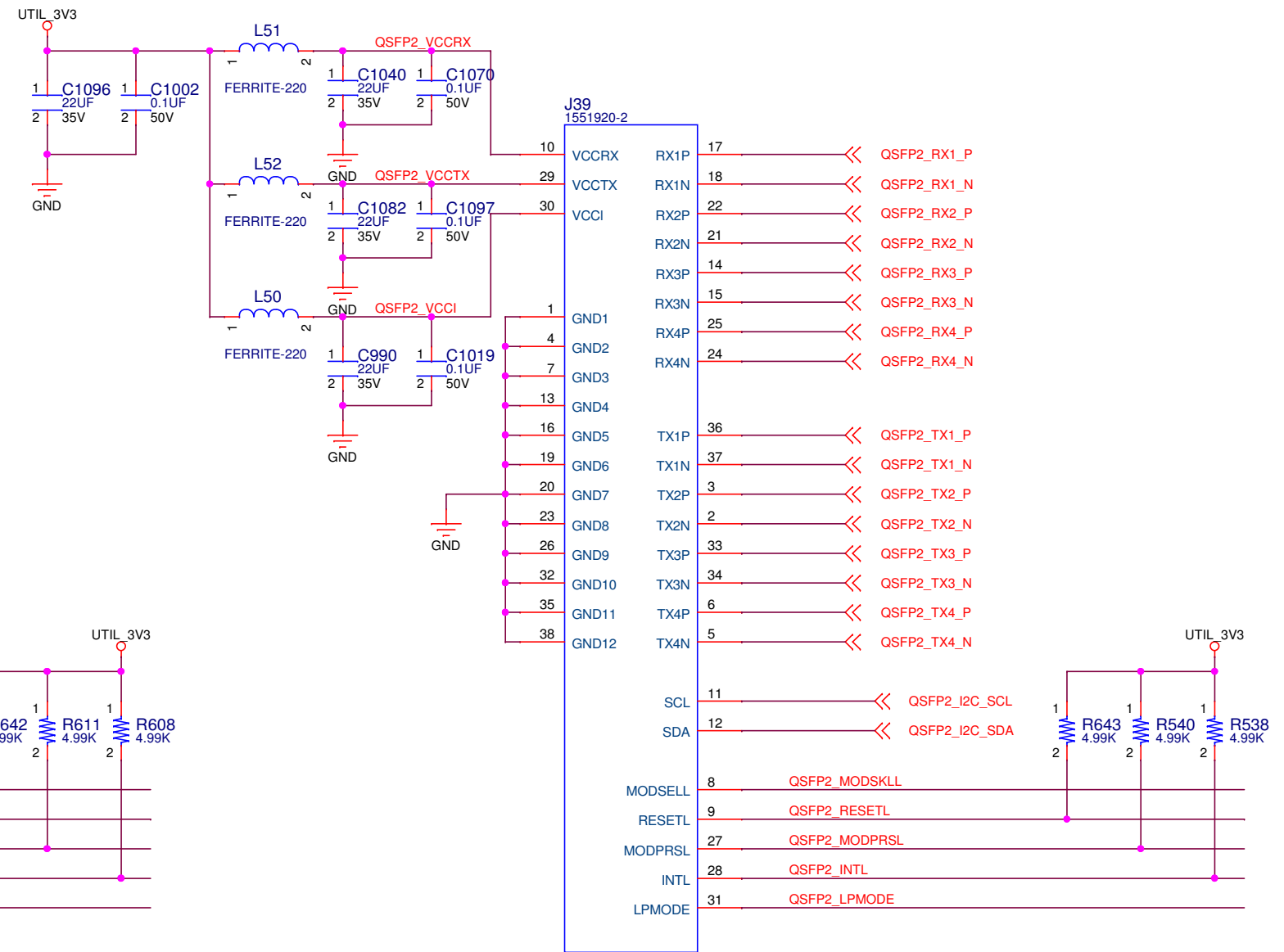
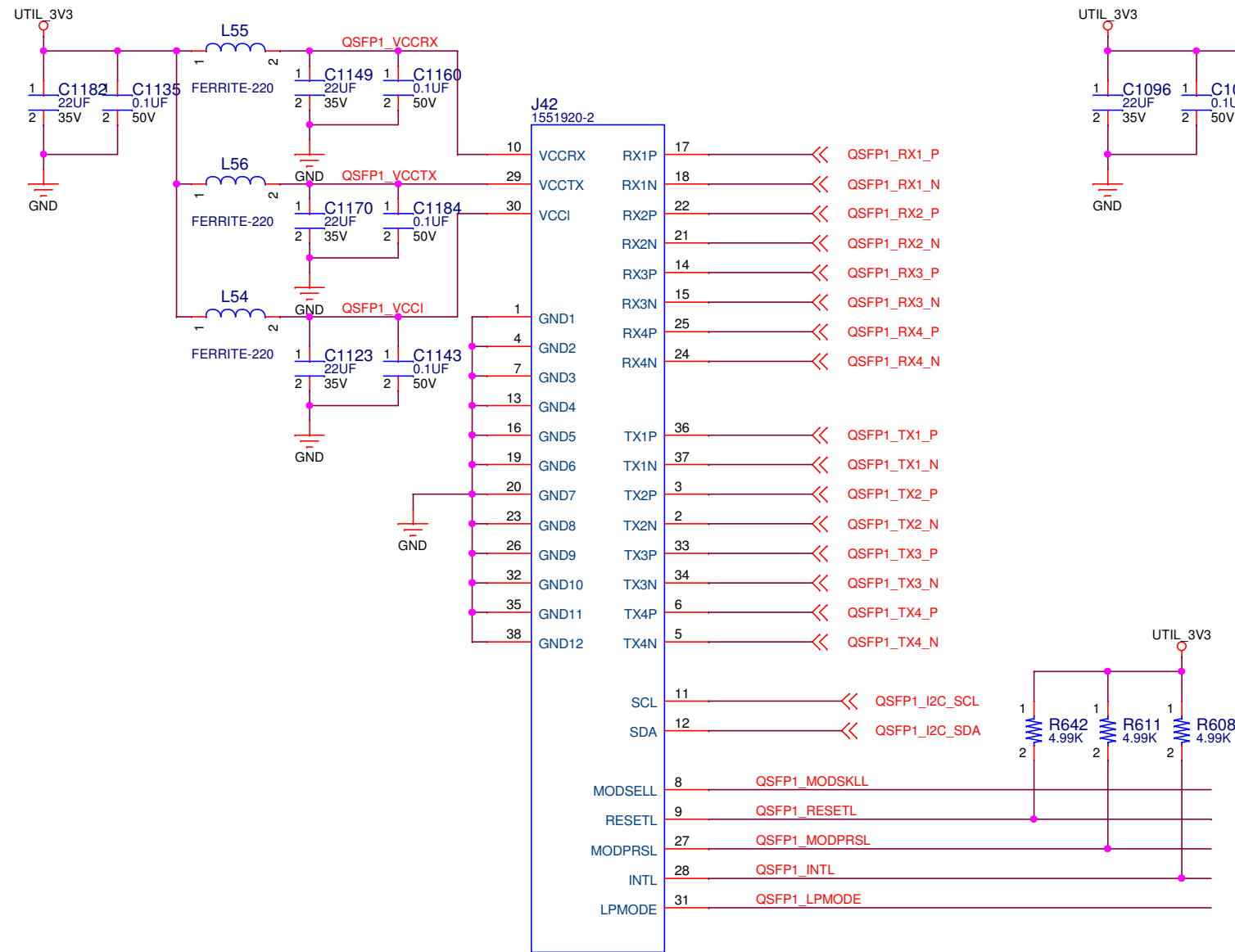
STRAP CONFIGURATION RESISTORS: SEE DP83867 DATASHEET



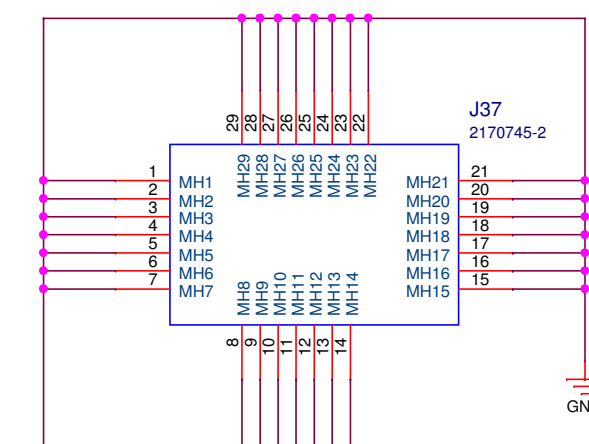
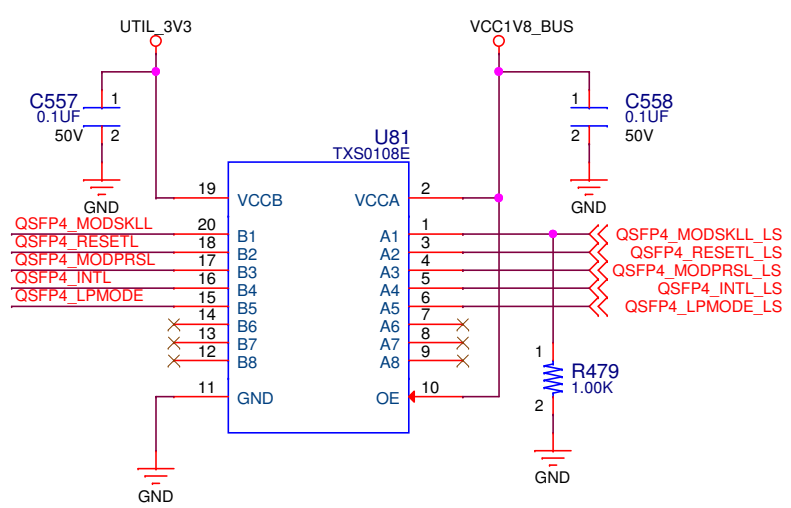
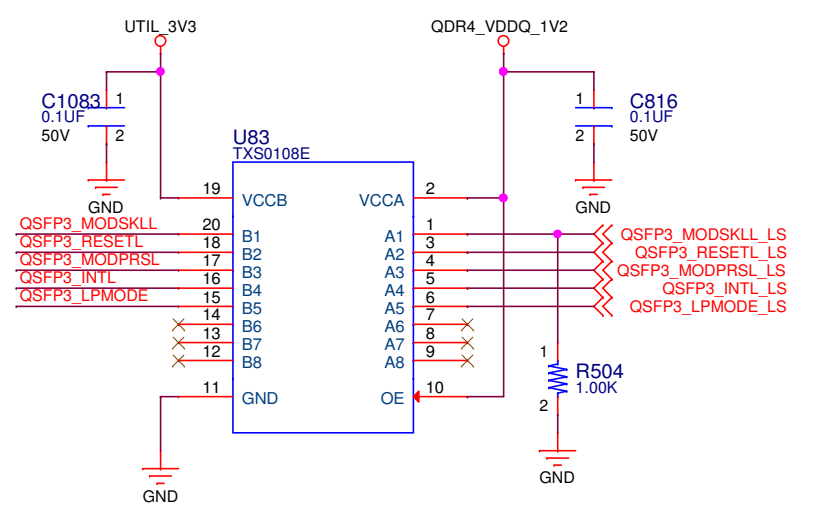
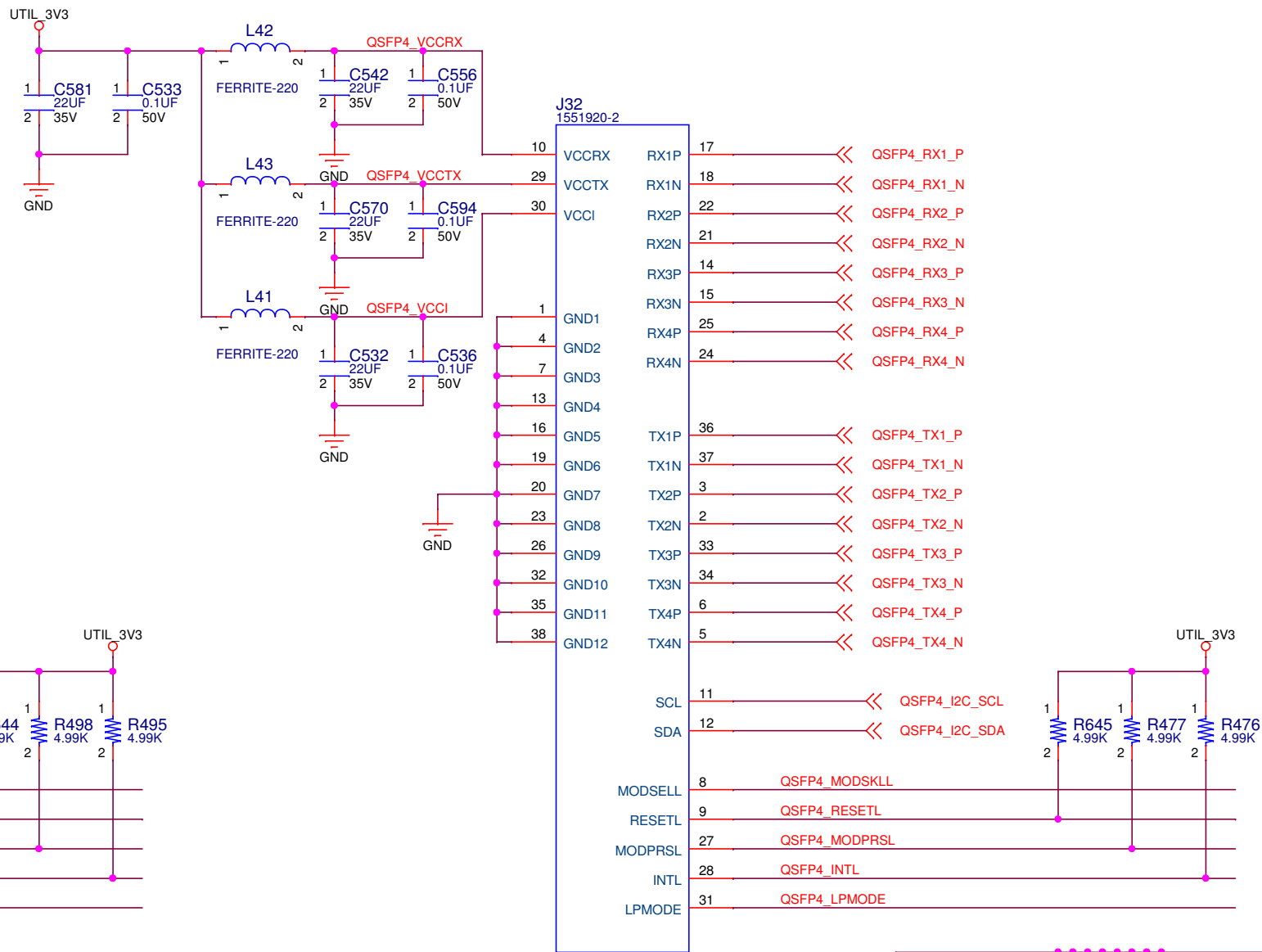
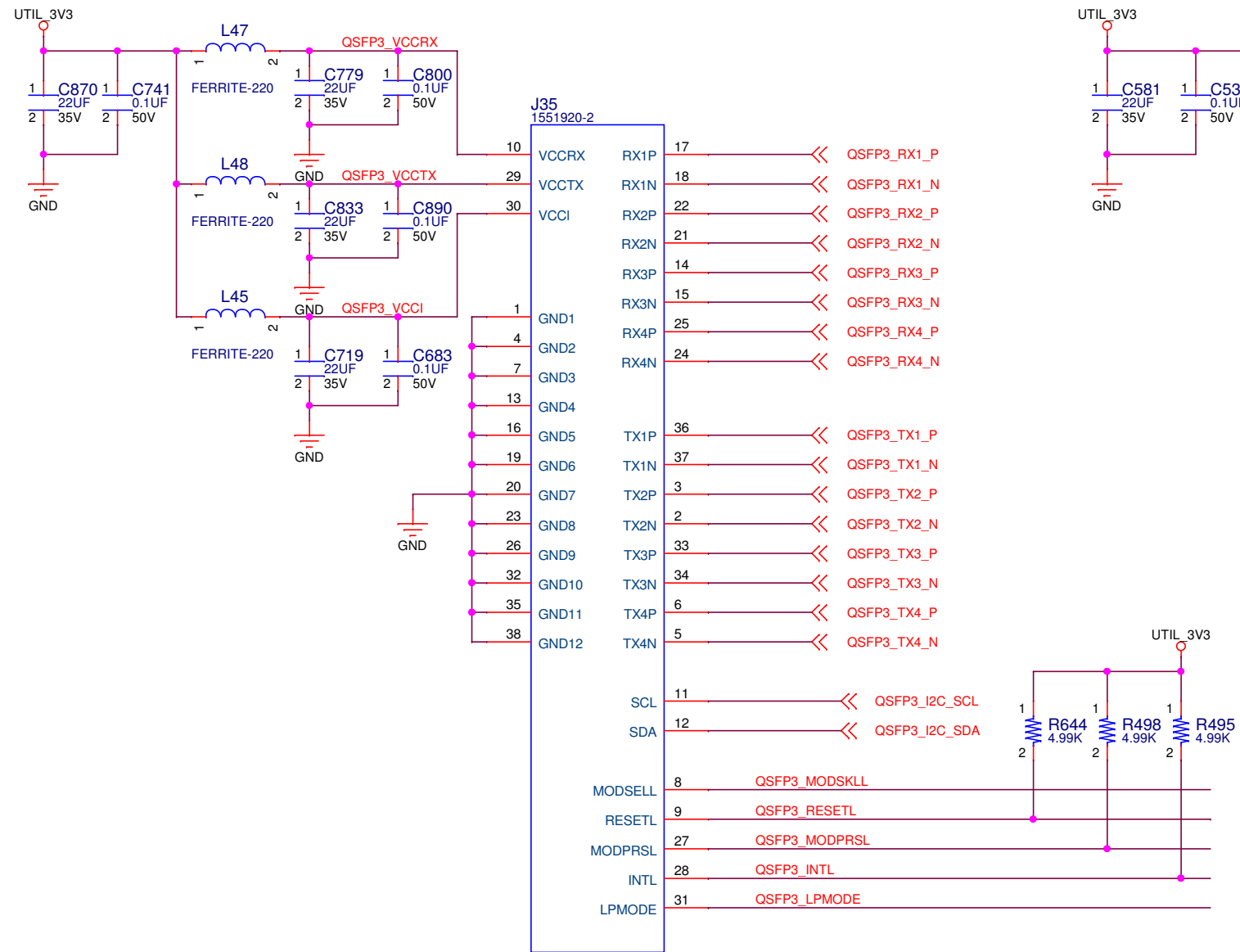
THESE CAPACITORS ARE PLACED AS CLOSE AS POSSIBLE TO THEIR RESPECTIVE DP83867 PINS



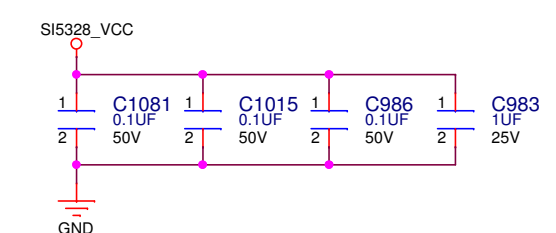
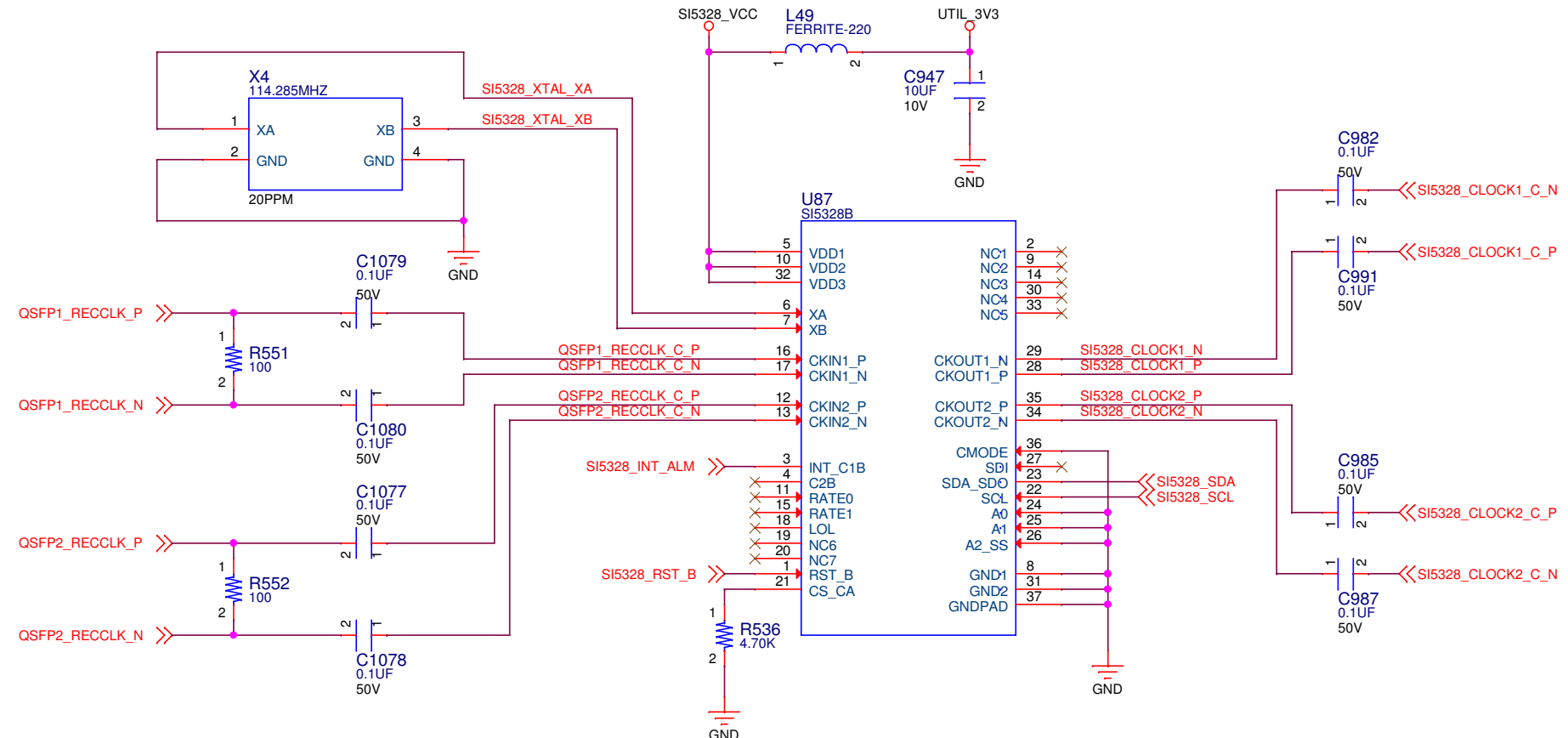
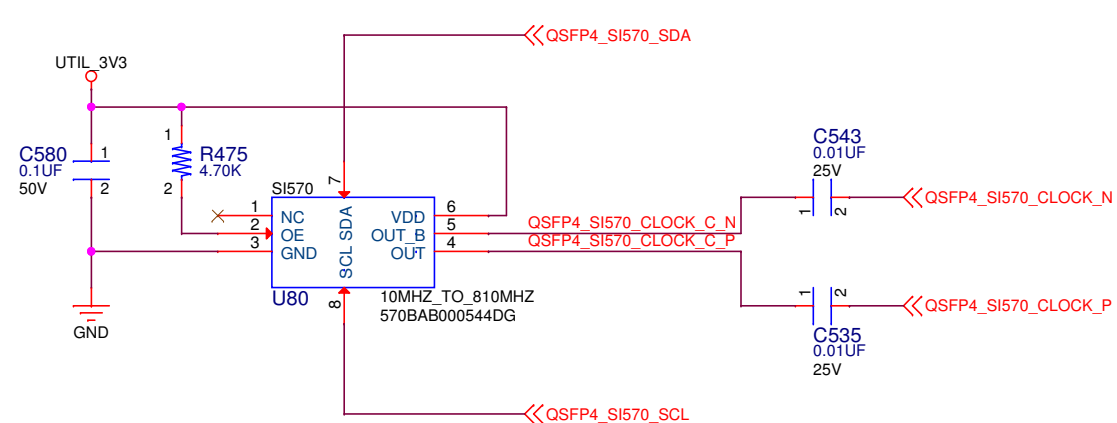
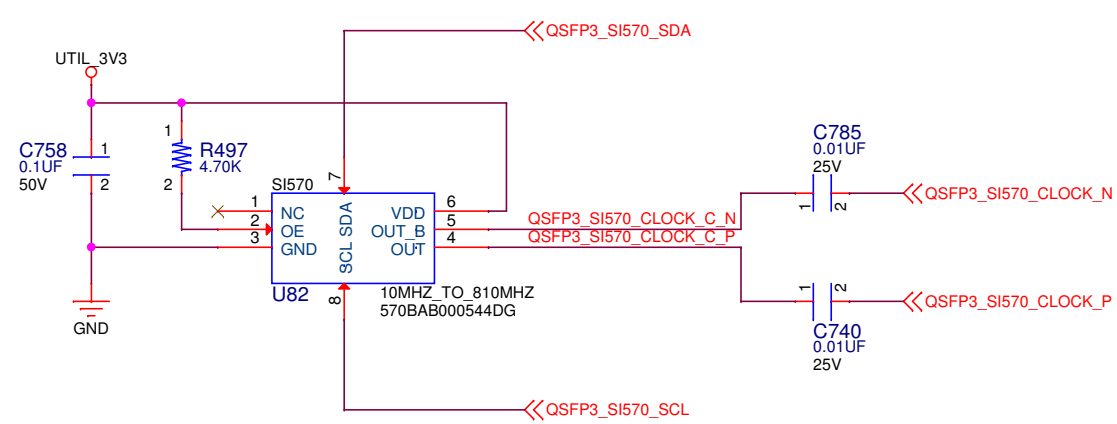
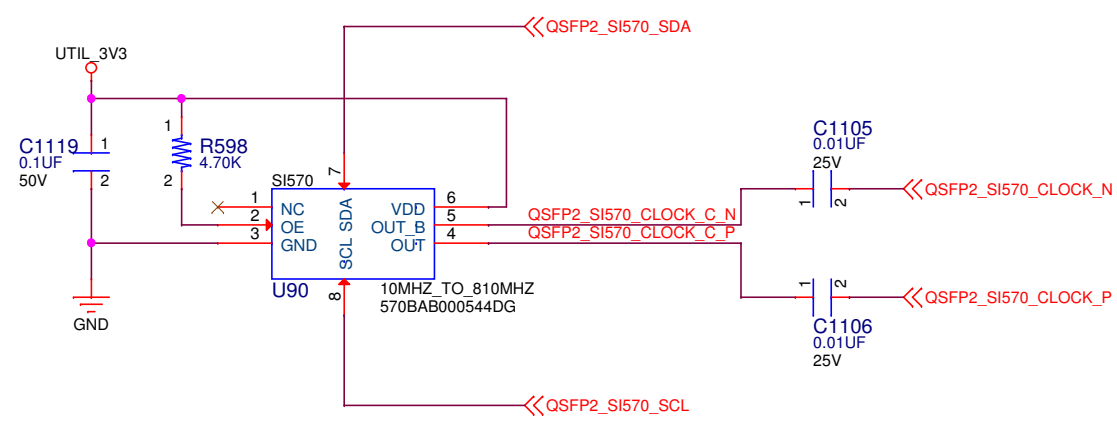
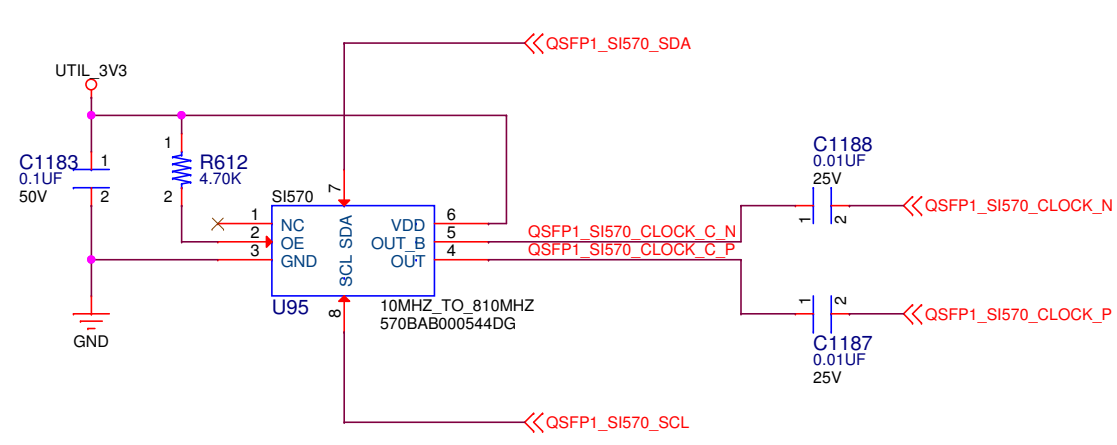
		PCB P/N : 1281016 ASSY P/N : 0432120 TEST P/N : TSS0201	
Title: HW-U1-VCU128 037 Ethernet SGMII			
Size B	Date Modified: Wednesday, October 10, 2018	Document Number: 0381852	Ver 1.0 Rev 01
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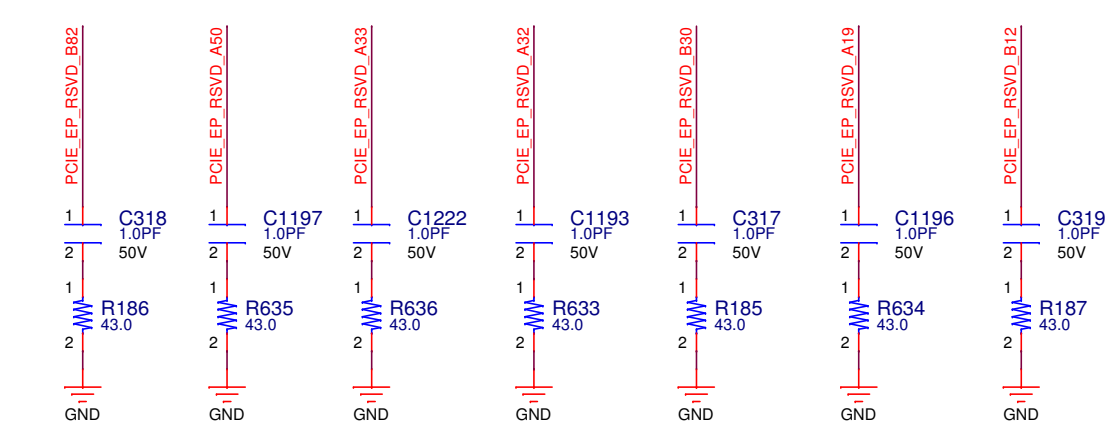
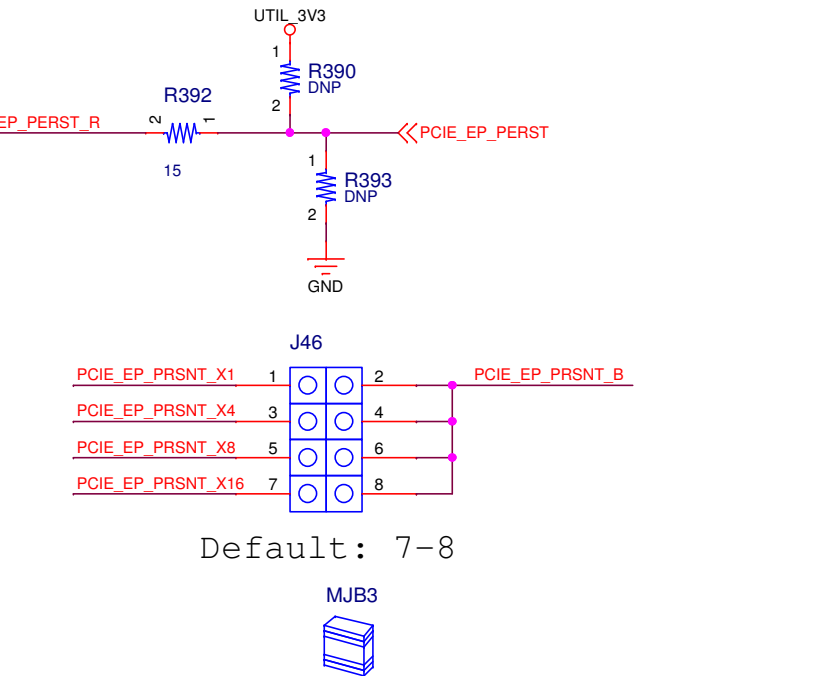
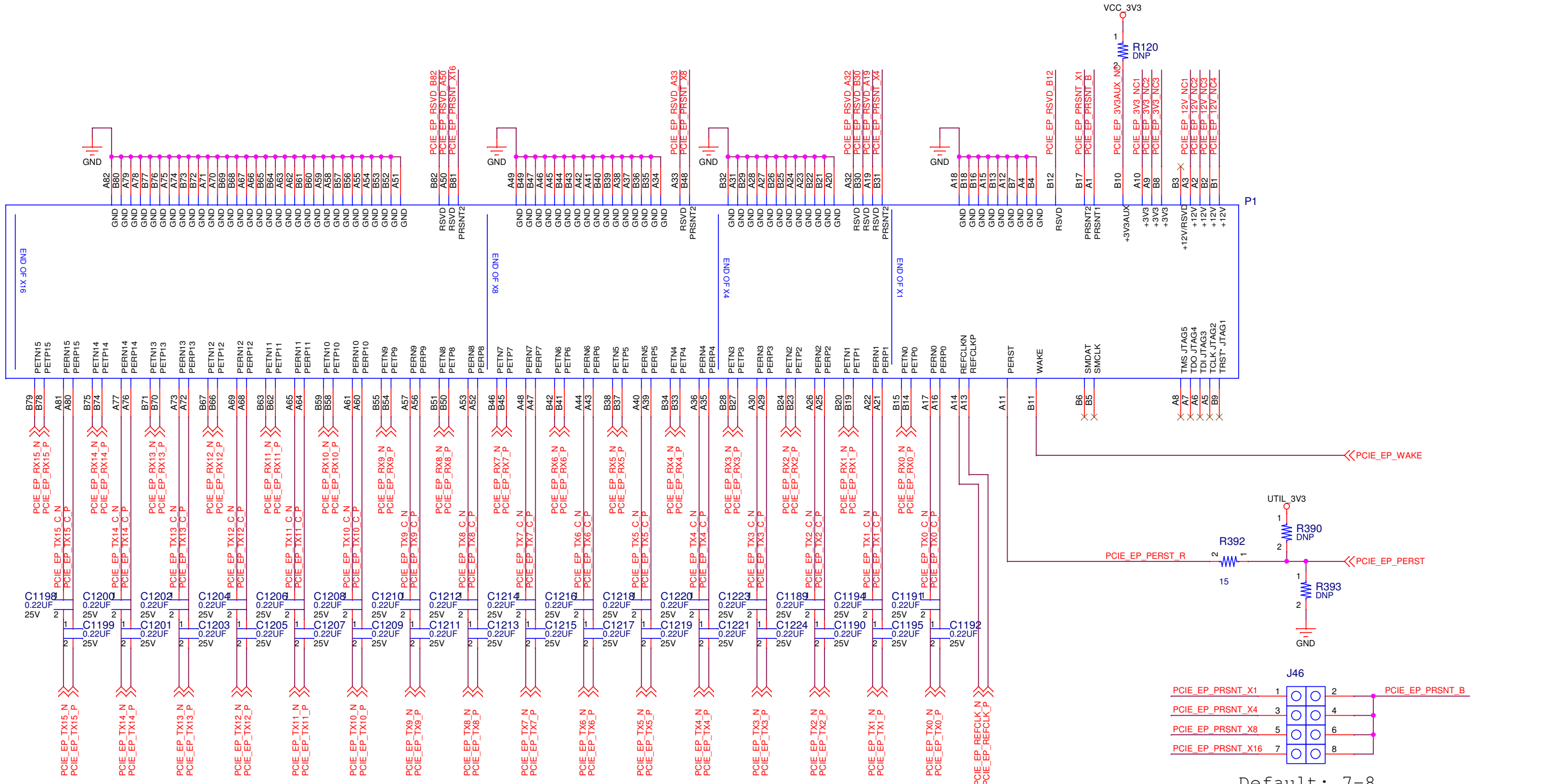
		PCB P/N : 1281016 ASSY P/N : 0432120 TEST P/N : TSS0201	
Title: HW-U1-VCU128 038 QSFP Connector 1 AND 2			
Size B	Date Modified: Wednesday, October 10, 2018	Document Number: 0381852	Ver 1.0 Rev 01
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		PCB P/N : 1281016 ASSY P/N : 0432120 TEST P/N : TSS0201	
Title: HW-U1-VCU128 039 QSFP Connector 3 AND 4			
Size B	Date Modified: Wednesday, October 10, 2018	Document Number: 0381852	Ver 1.0 Rev 01
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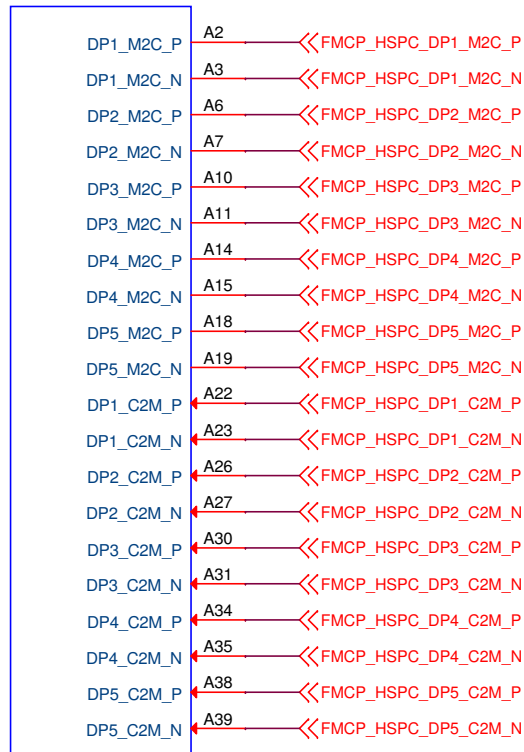


		PCB P/N : 1281016 ASSY P/N : 0432120 TEST P/N : TSS0201	
Title: HW-U1-VCU128 040 QSFP Clocks			
Size B	Date Modified: Wednesday, October 10, 2018	Document Number: 0381852	Ver 1.0 Rev 01
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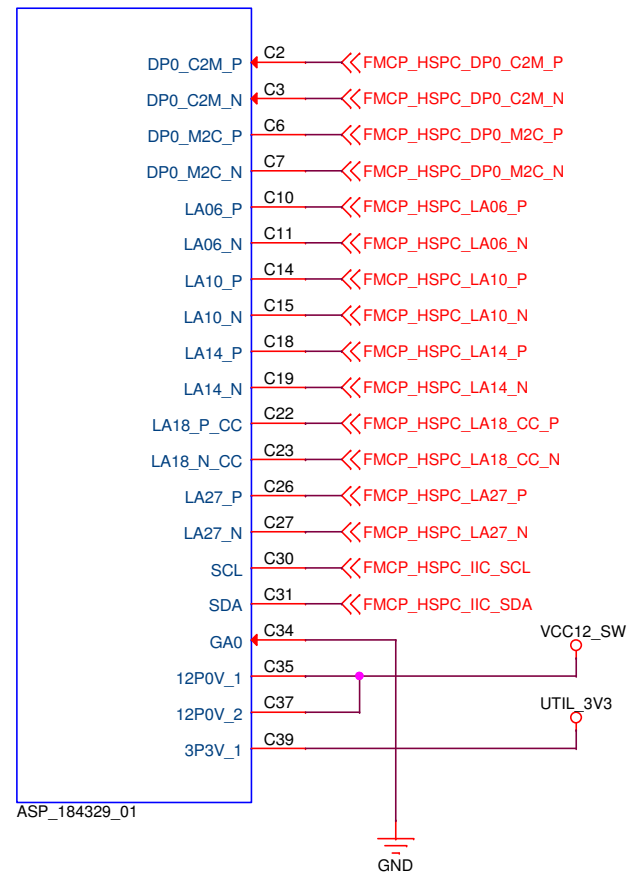


		PCB P/N : 1281016 ASSY P/N : 0432120 TEST P/N : TSS0201	
Title: HW-U1-VCU128 041 PCIe Endpoint Edge Conn.			
Size B	Date Modified: Wednesday, October 10, 2018	Document Number: 0381852	Ver 1.0 Rev 01
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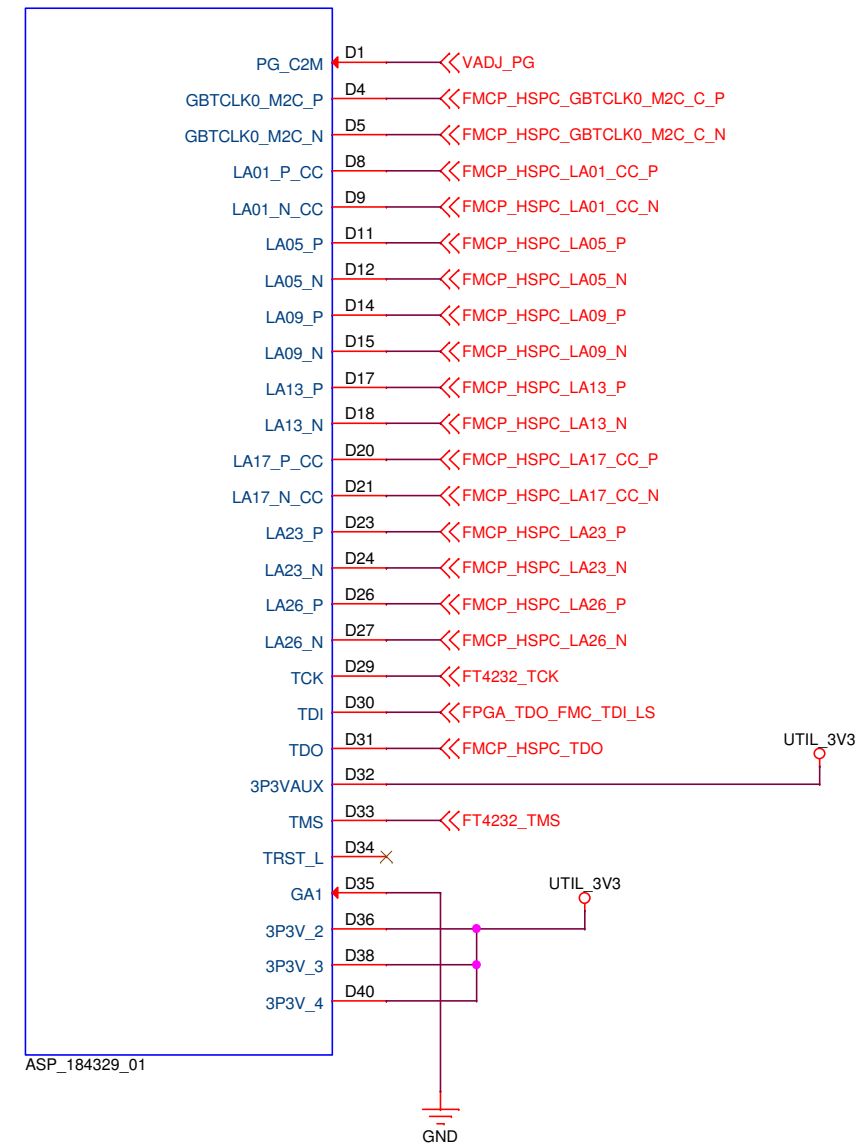
J18A



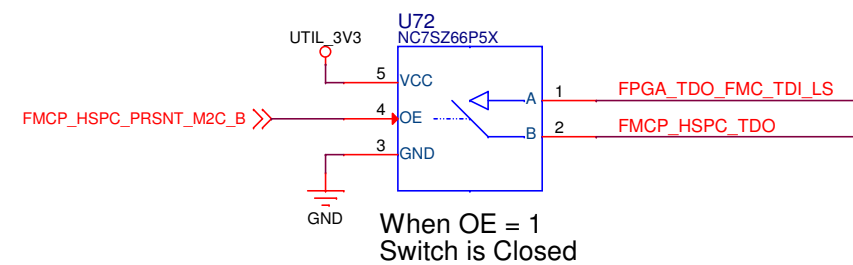
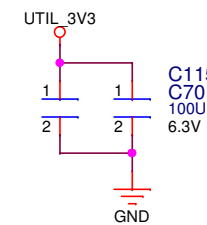
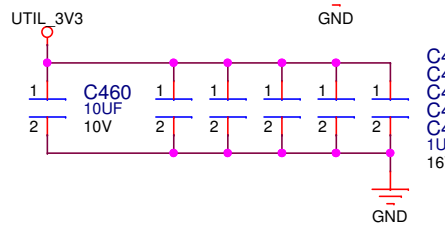
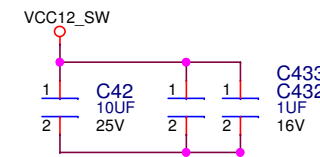
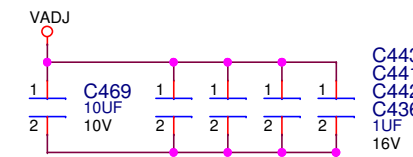
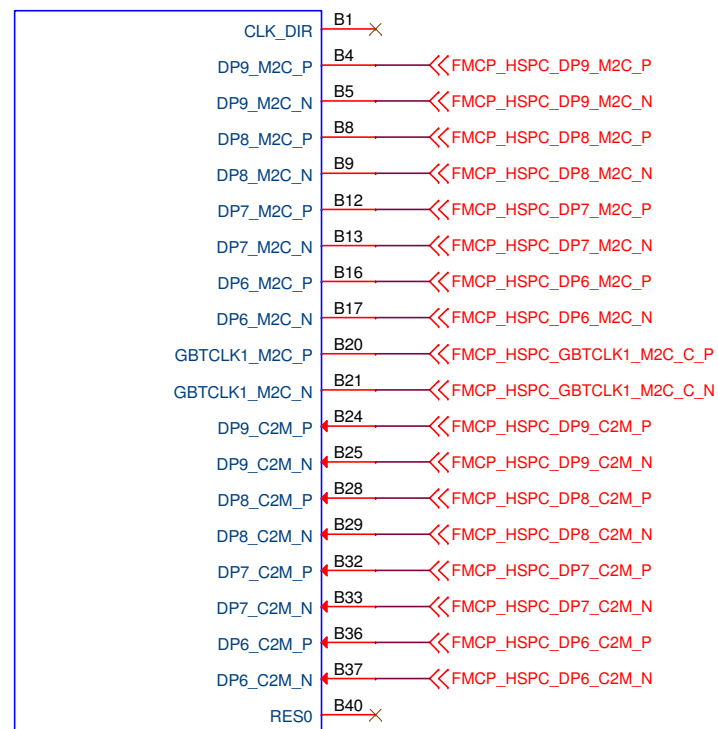
J18C



J18D

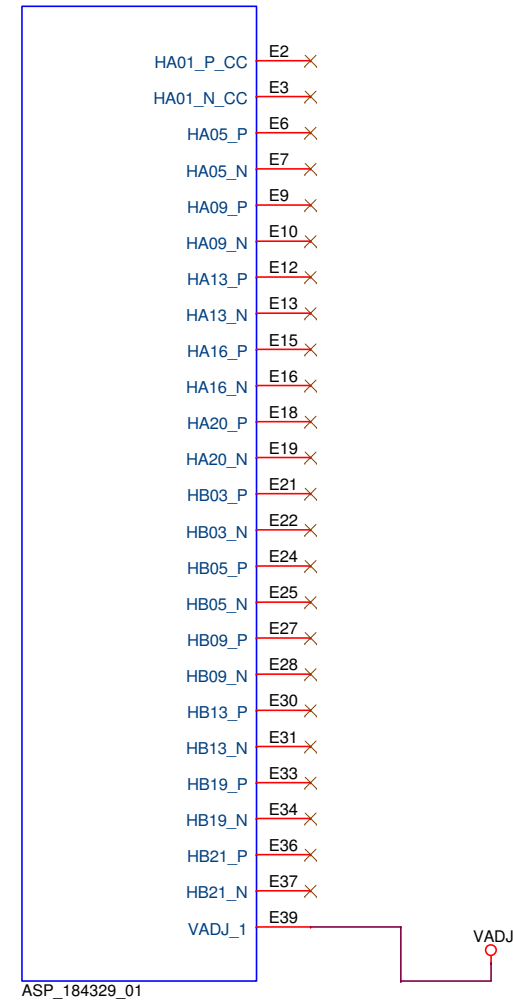


J18B

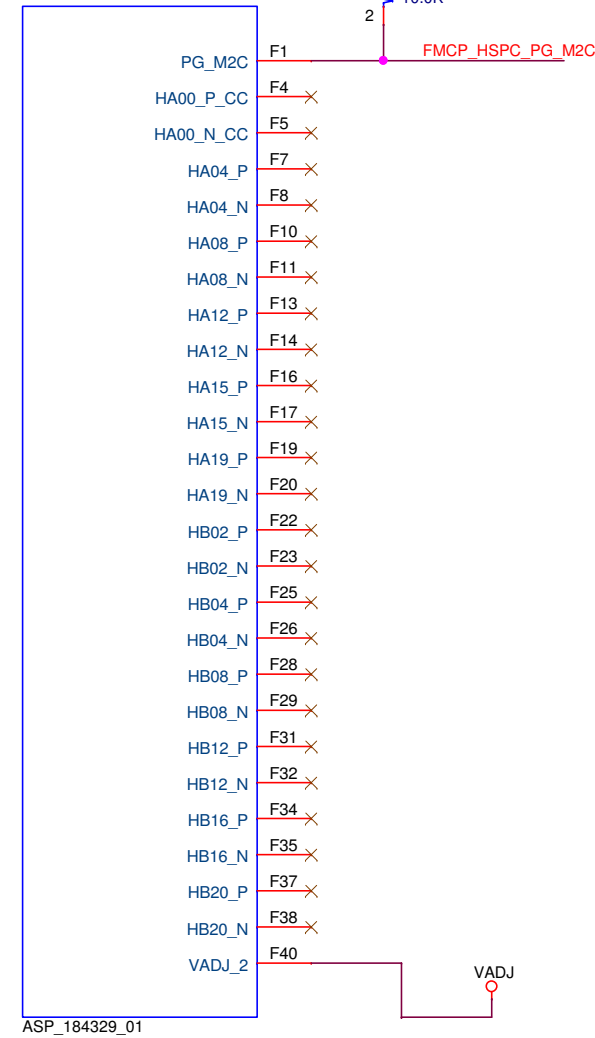


		PCB P/N : 1281016 ASSY P/N : 0432120 TEST P/N : TSS0201	
Title: HW-U1-VCU128 042 FMC HSPC1			
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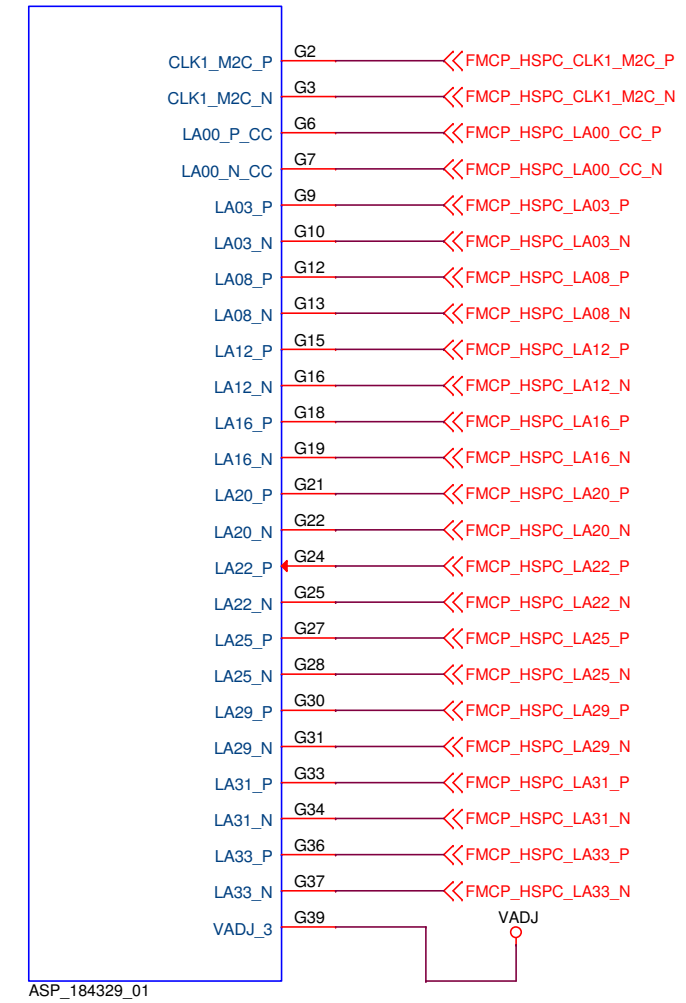
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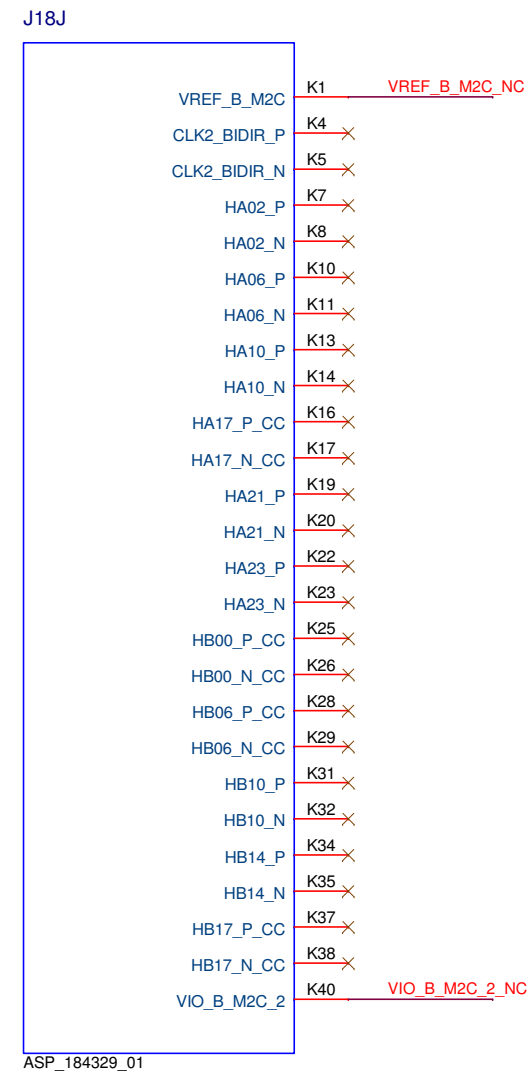
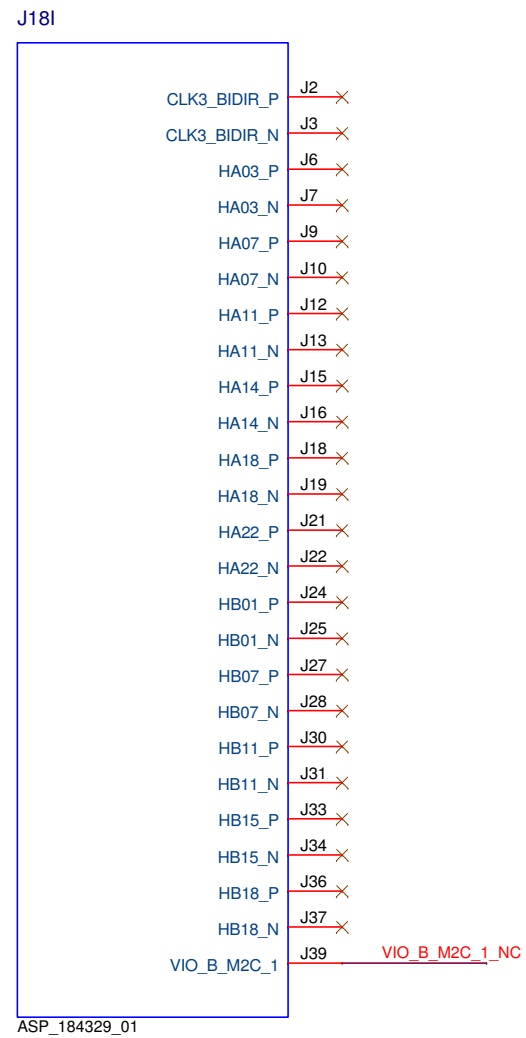
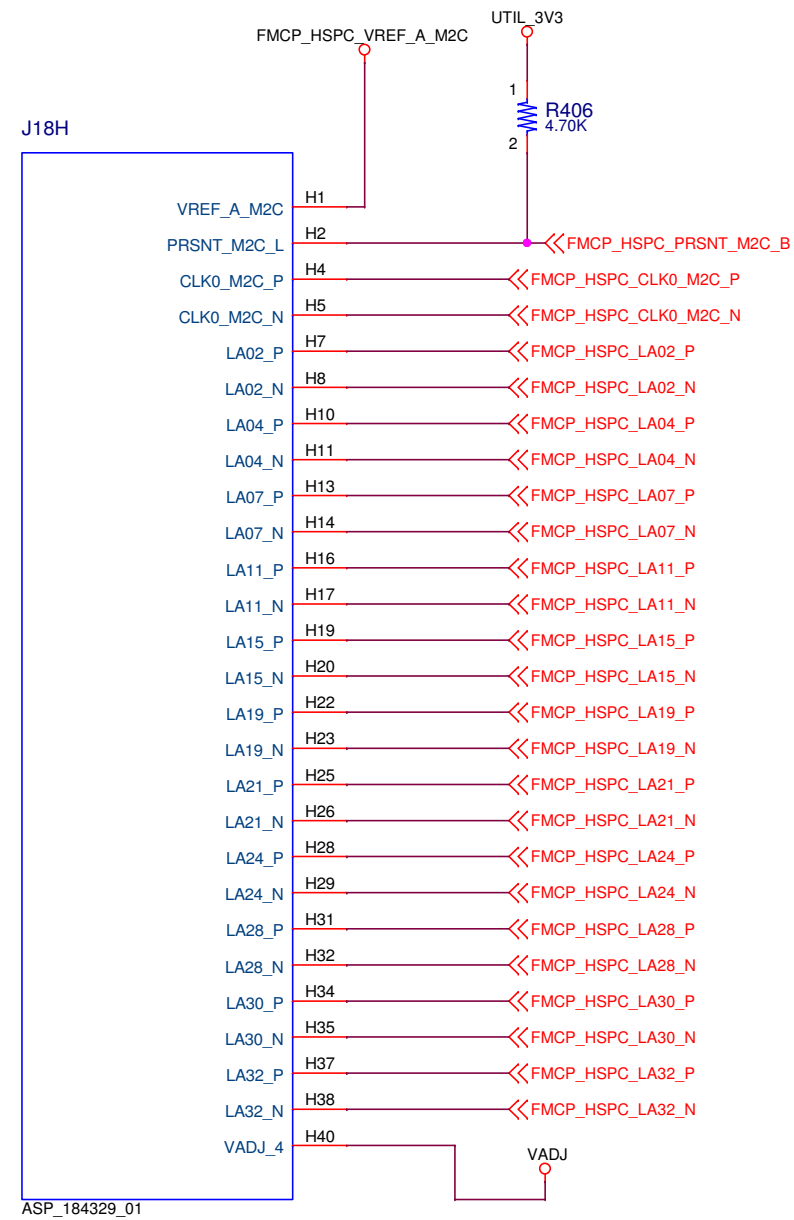
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J18G

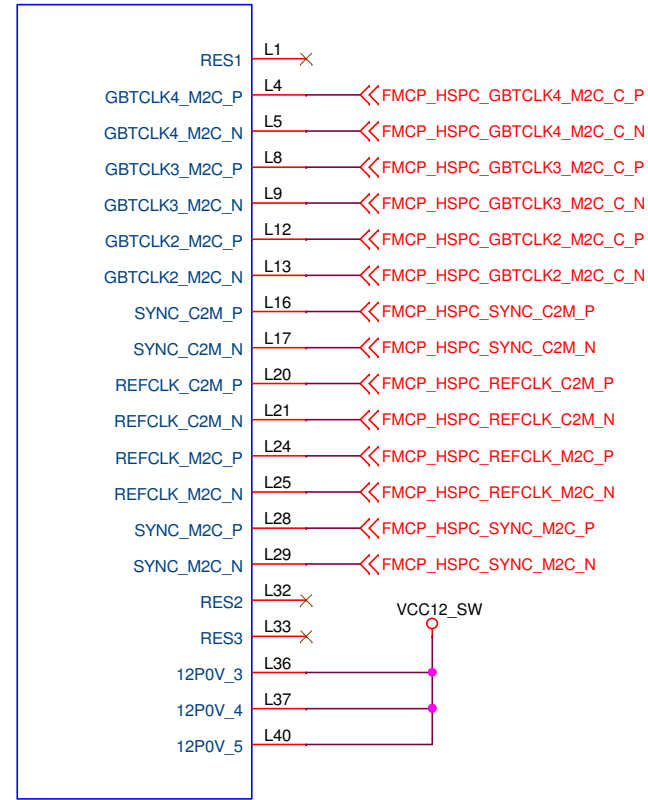


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Title: HW-U1-VCU128 043 FMC HSPC2			
Size	Date Modified:	Document Number:	Ver
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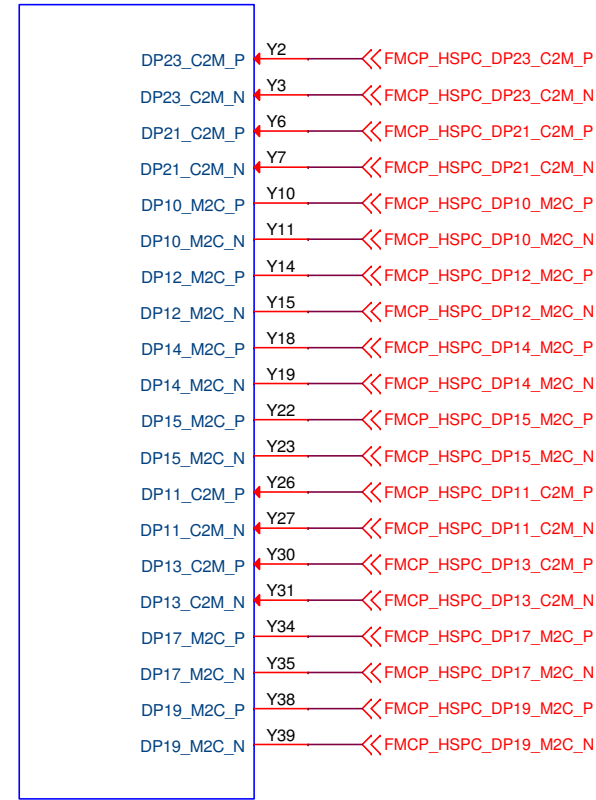
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Title: HW-U1-VCU128 044 FMC HSPC3			
Size B	Date Modified: Wednesday, October 10, 2018	Document Number: 0381852	Ver 1.0 Rev 01
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J18K



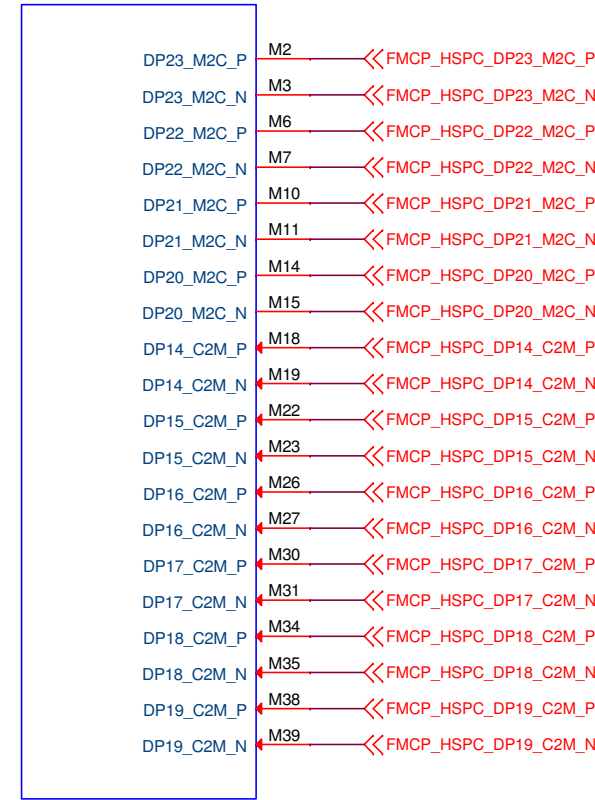
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J18L



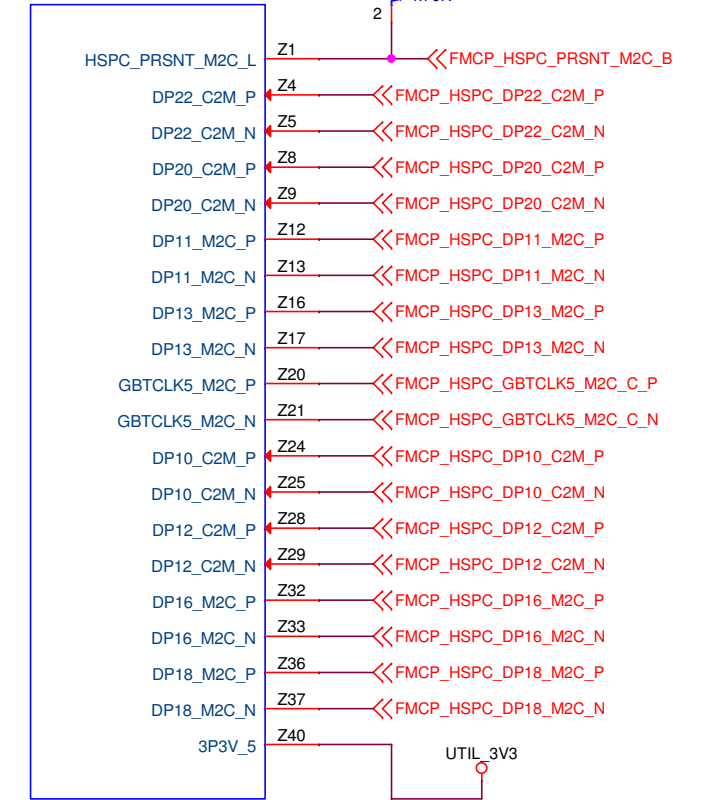
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J18M



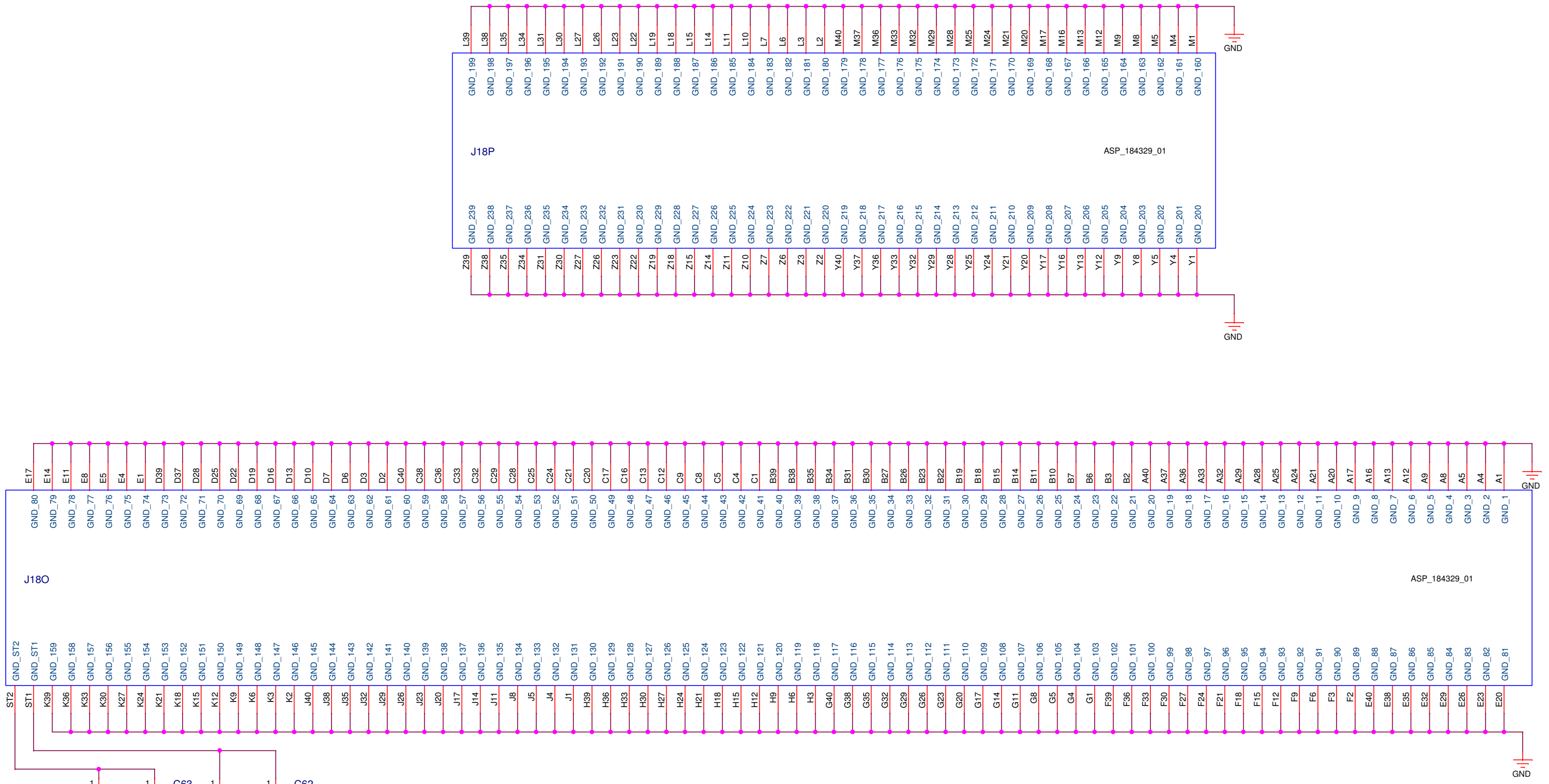
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J18N

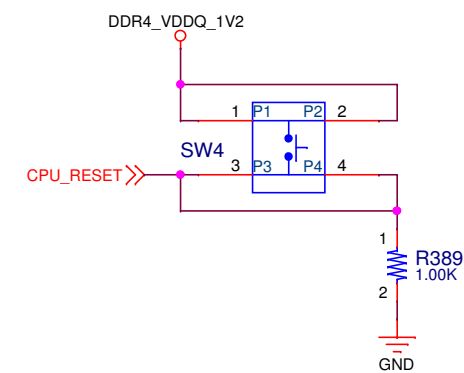
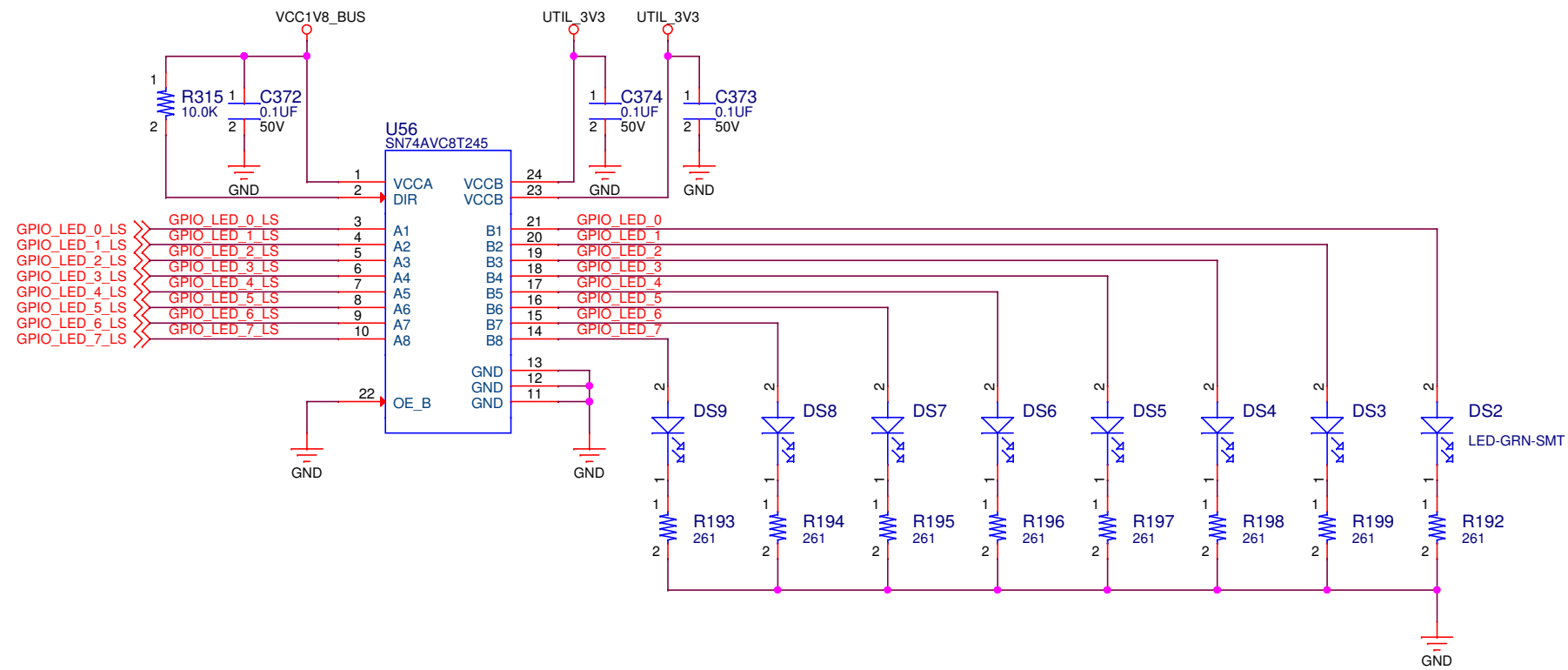


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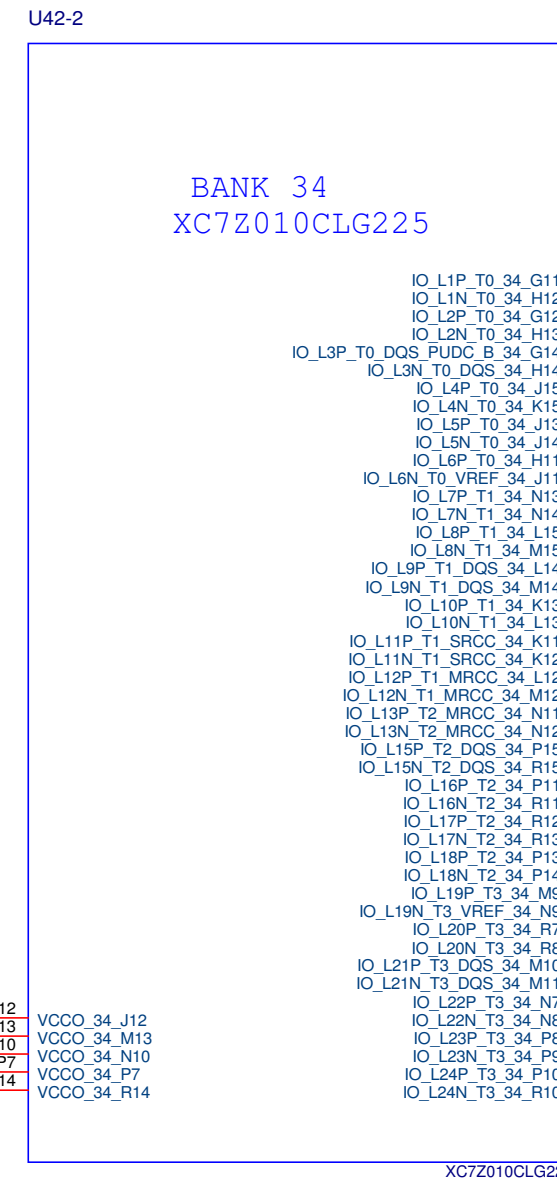
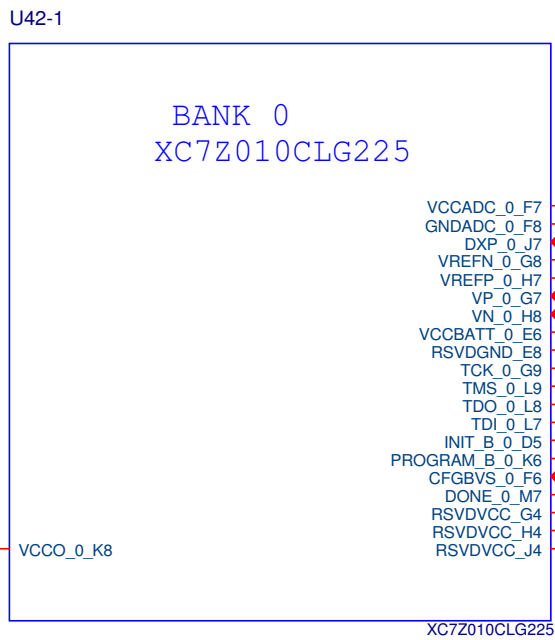
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Title: HW-U1-VCU128 045 FMC HSPC4			
Size	Date Modified:	Document Number:	Ver
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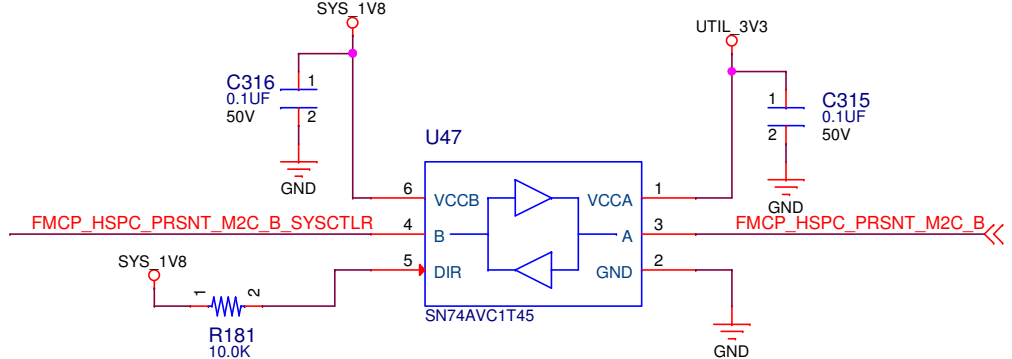
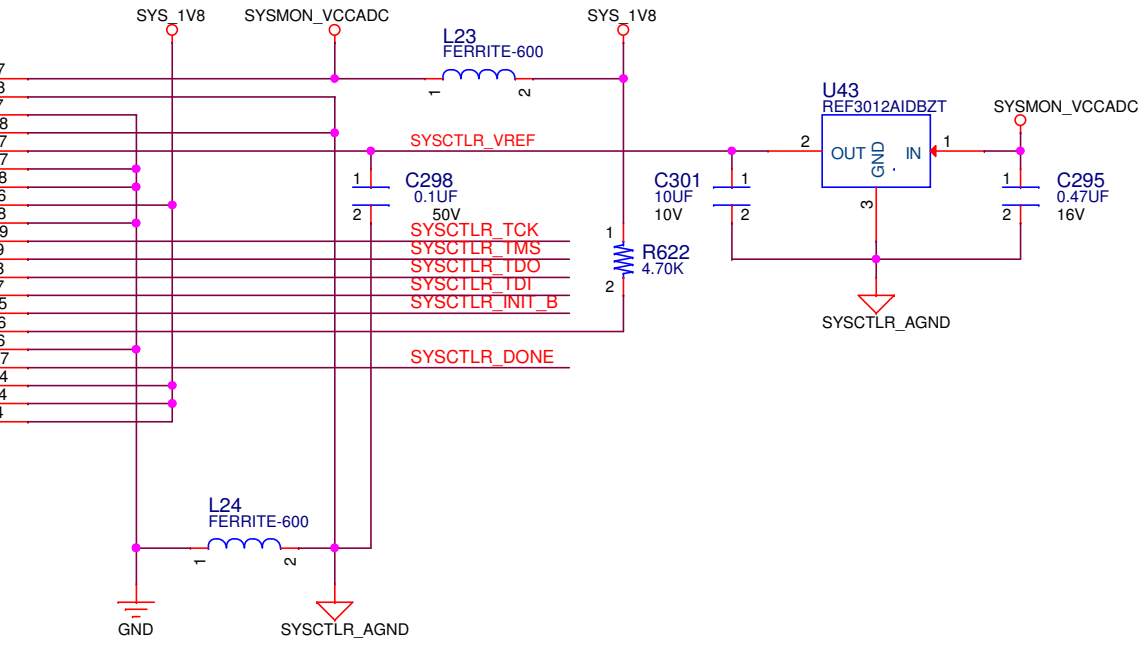
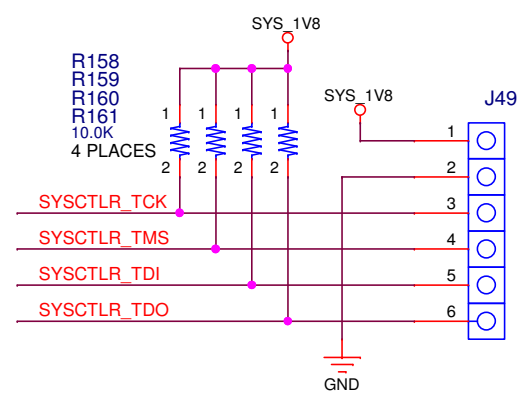
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Title: HW-U1-VCU128 046 FMC HSPC5			
Size B	Date Modified: Wednesday, October 10, 2018	Document Number: 0381852	Ver 1.0 Rev 01
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		PCB P/N : 1281016 ASSY P/N : 0432120 TEST P/N : TSS0201	
Title: HW-U1-VCU128 047 GPIO LEDs Switches Buttons			
Size	Date Modified:	Document Number:	Ver
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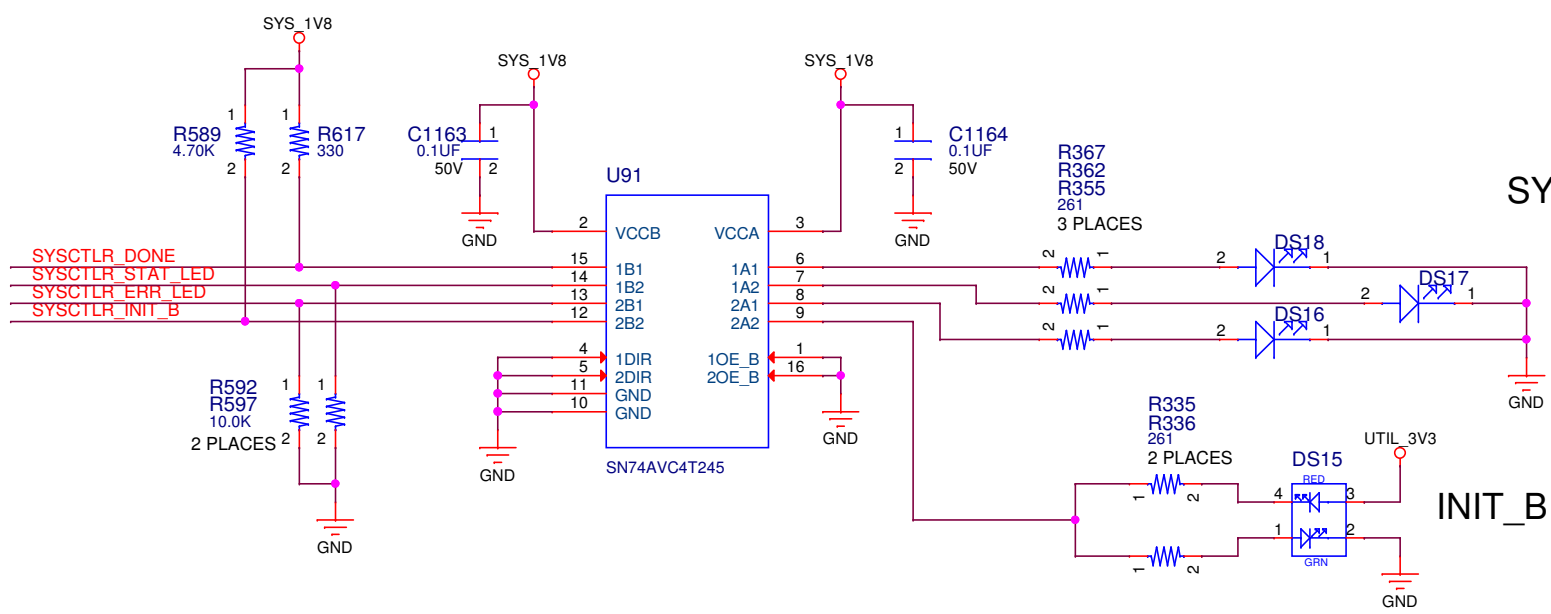


**SYSTEM CONTROLLER
JTAG / DEBUG CABLE**

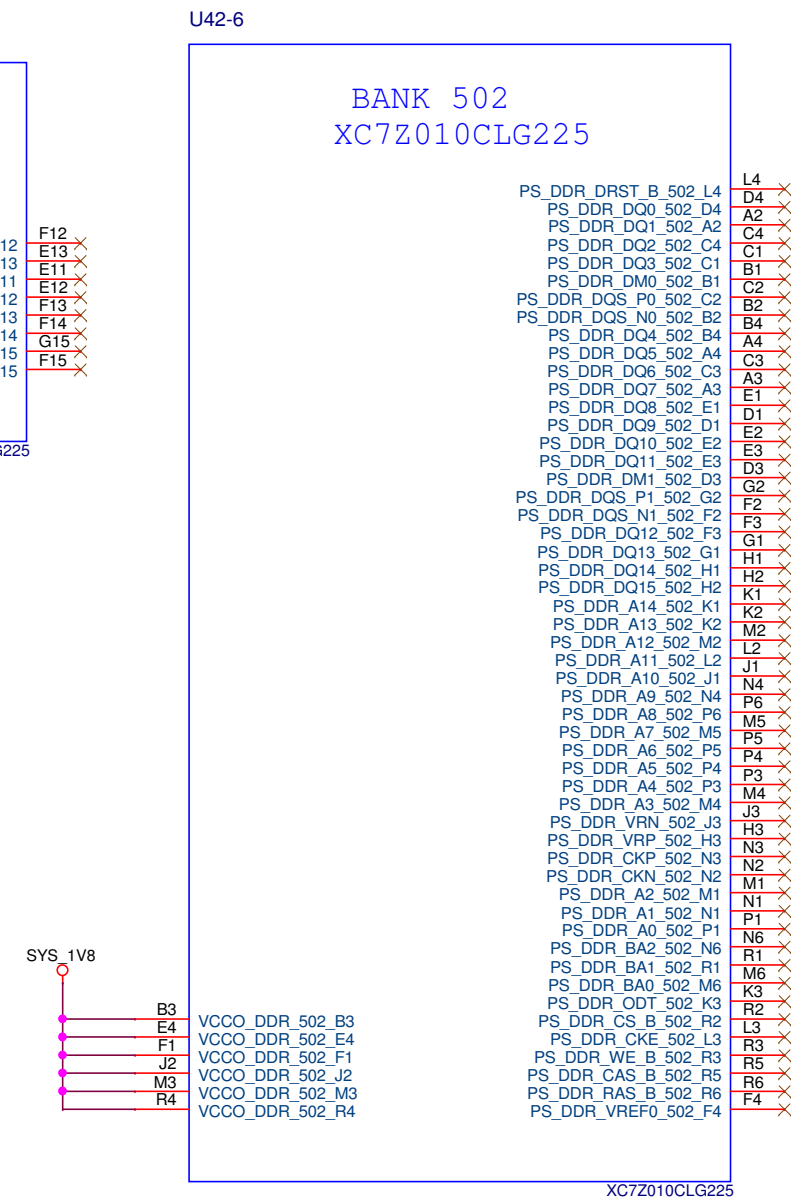
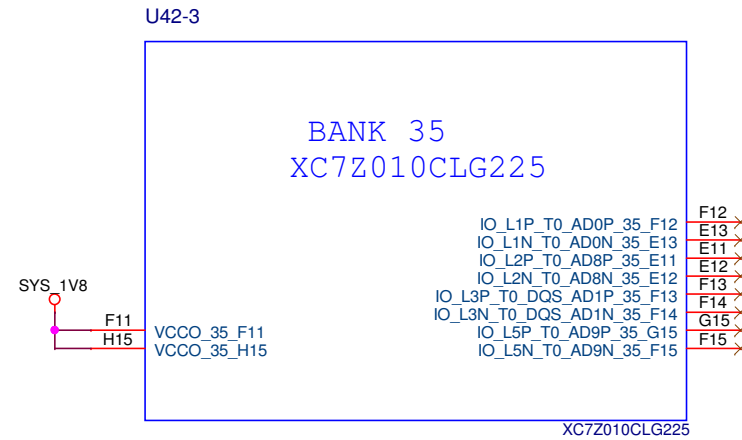


SYSTEM CONTROLLER

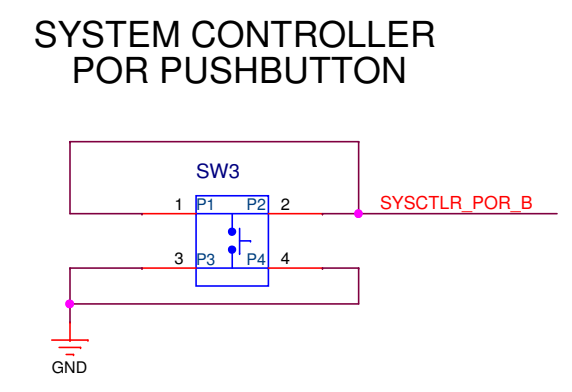
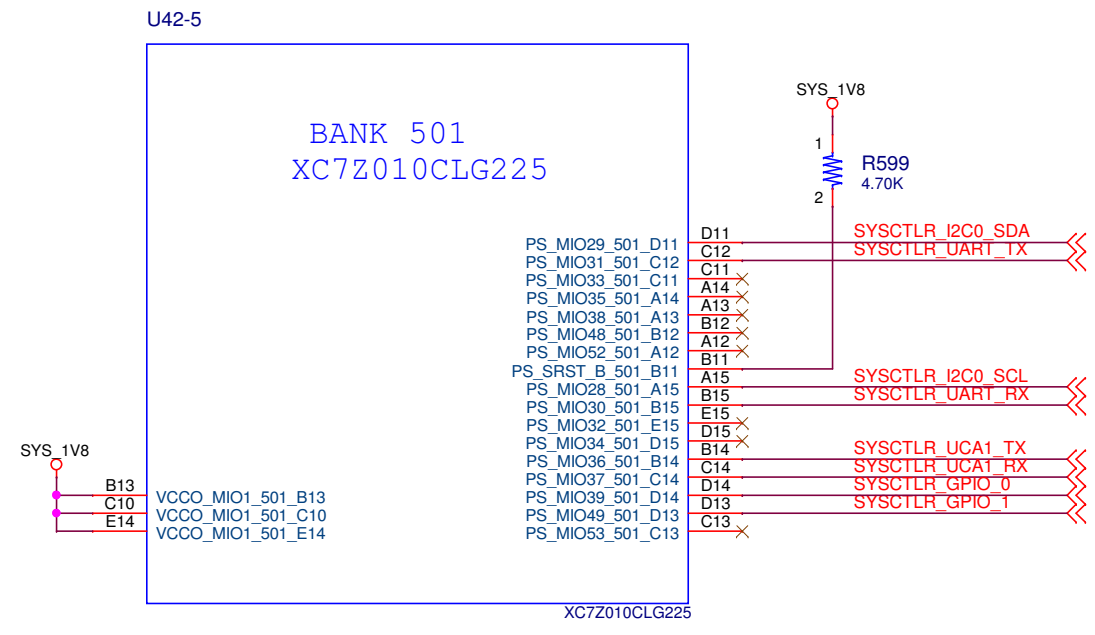
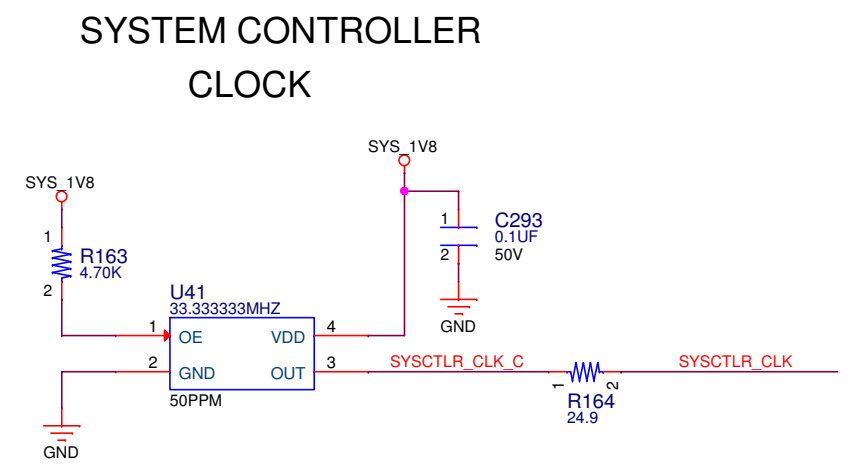
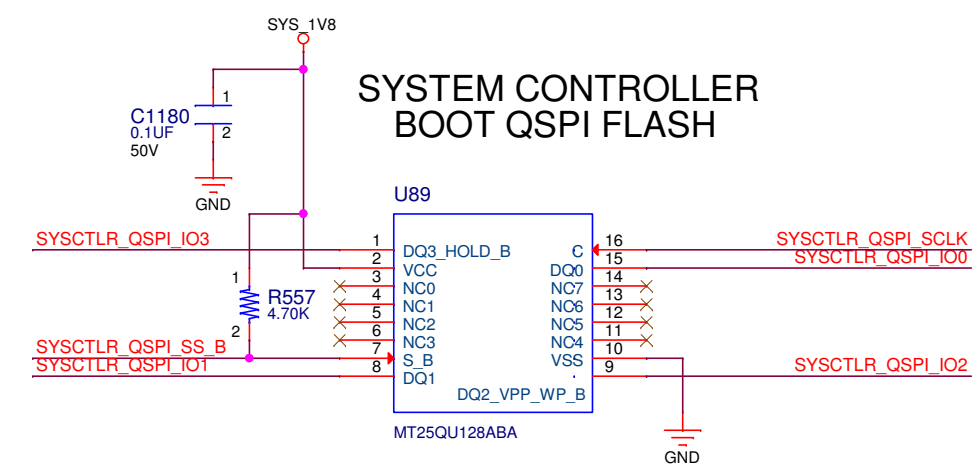
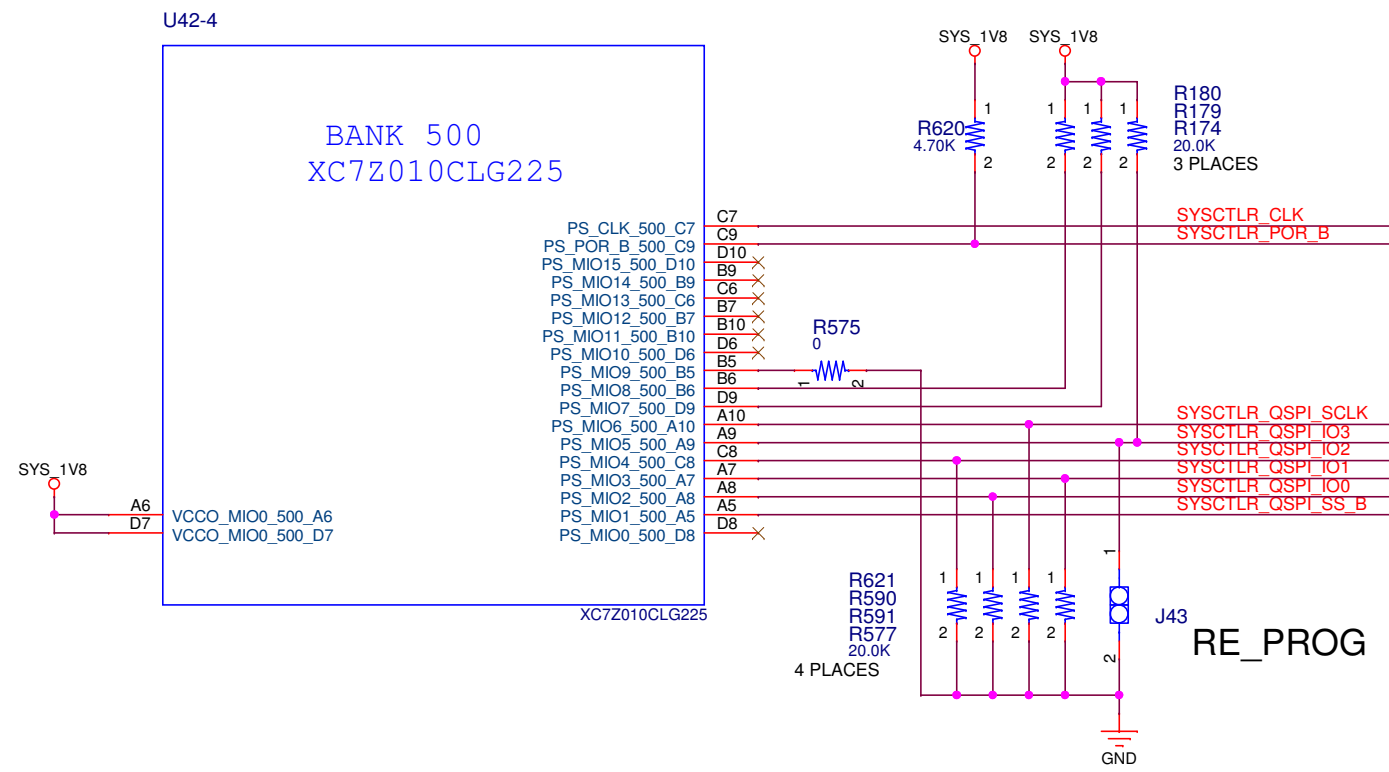
**DONE
STATUS
ERROR (RED)**



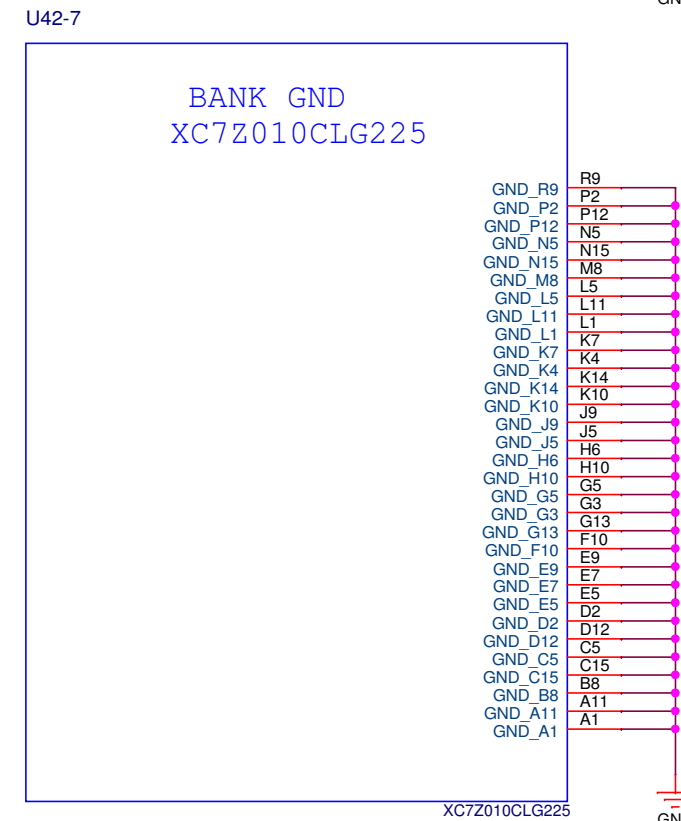
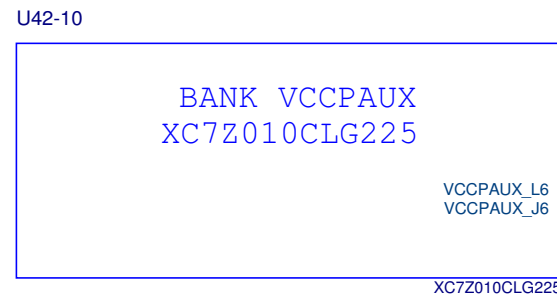
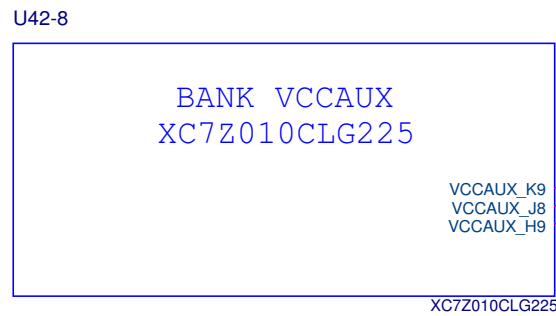
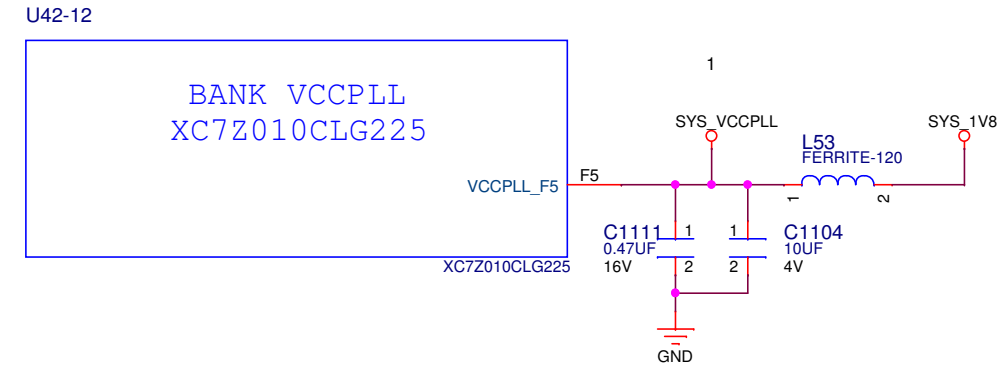
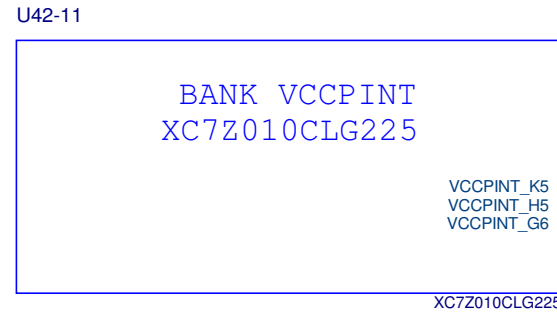
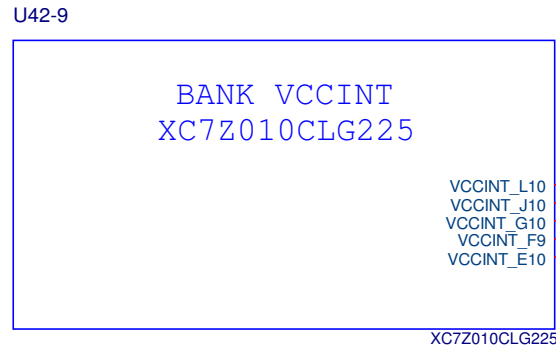
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Title: HW-U1-VCU128 048 SYSCTRL BANK 0 CONFIG/JTAG			
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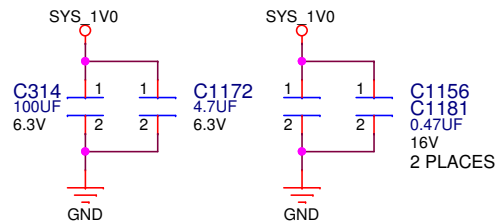
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Title: HW-U1-VCU128 049 SYSCTRL BANKS 35/502 I/O			
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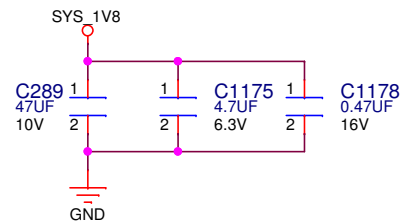
		PCB P/N : 1281016 ASSY P/N : 0432120 TEST P/N : TSS0201	
Title: HW-U1-VCU128 050 SYSCTRL BANK 500 SD/QSPI/SW			
Size B	Date Modified: Wednesday, October 10, 2018	Document Number: 0381852	Ver 1.0 Rev 01
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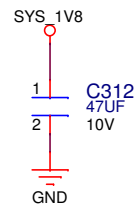
VCCINT/VCCBRAM



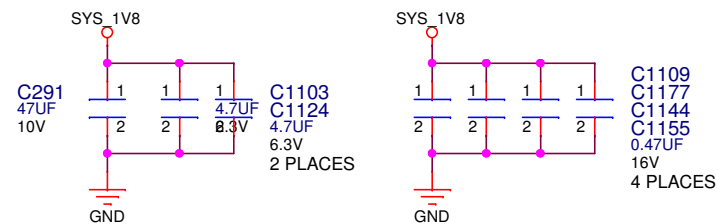
VCCAUX



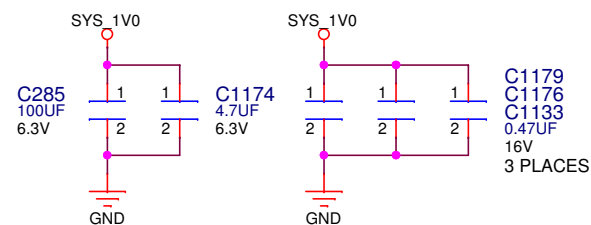
BANK 0



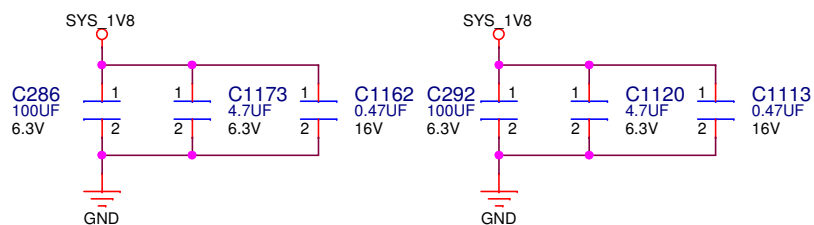
BANK 34



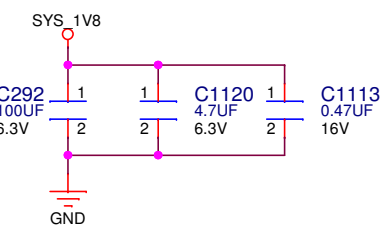
VCCPINT



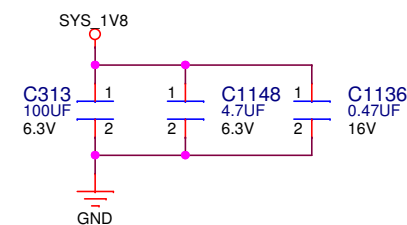
VCCPAUX



VCCO_MIO0



VCCO_MIO1



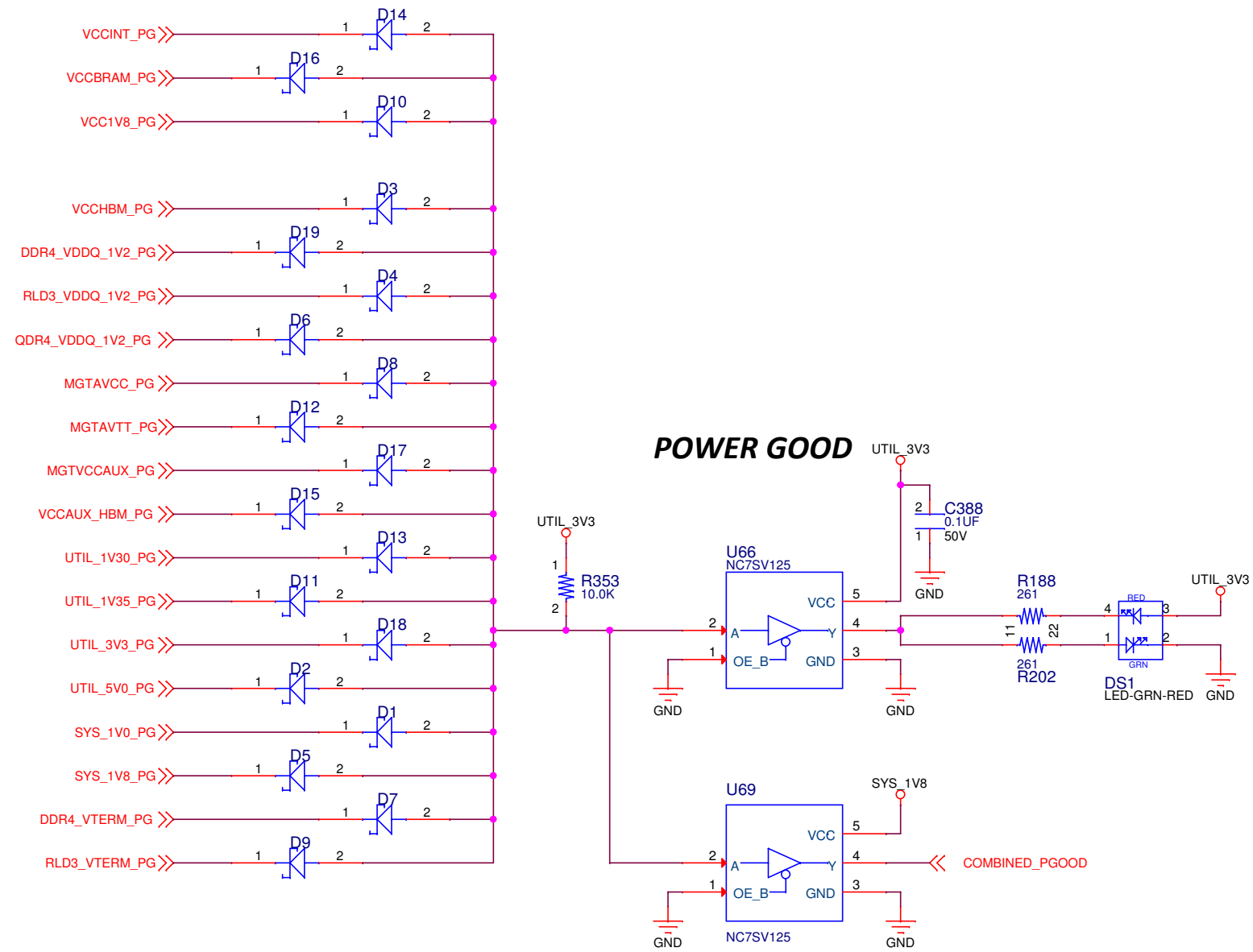
XILINX
2100 All Programmable Drive
San Jose, CA 95124

PCB P/N : 1281016
ASSY P/N : 0432120
TEST P/N : TSS0201

Title: HW-U1-VCU128
051 SYSCTRL PWR CONN DECOUPLING

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Engineer: RO			Rev 01

1 REVIEW VCCPLL - PS PLL SUPPLY SECTION IN XILINX UG933 PRIOR TO ROUTING SYS_VCCPLL POWER CONNECTION.

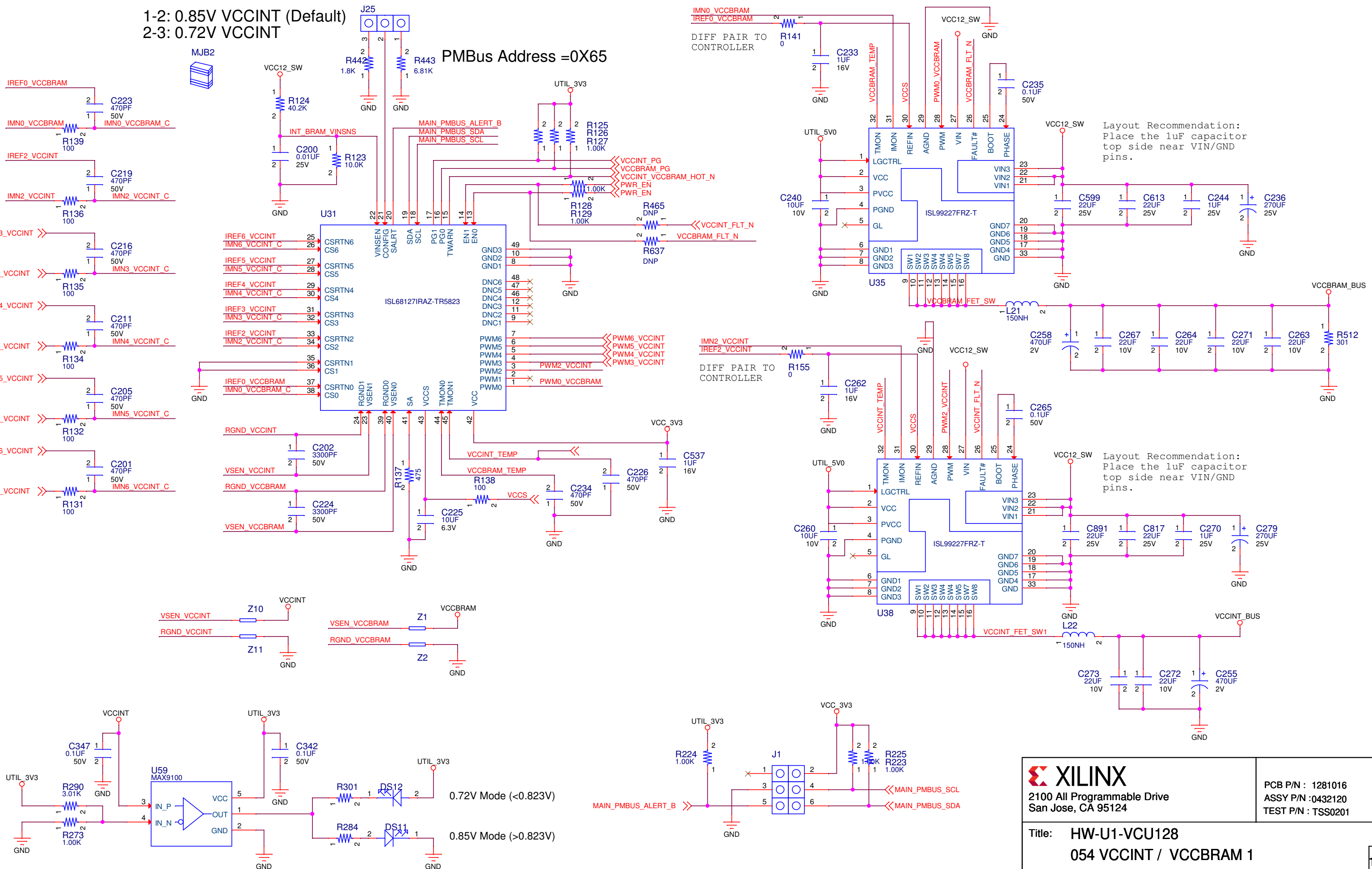


		PCB P/N : 1281016 ASSY P/N : 0432120 TEST P/N : TSS0201	
Title: HW-U1-VCU128 053 Power Good LED			
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1-2: 0.85V VCCINT (Default)
2-3: 0.72V VCCINT

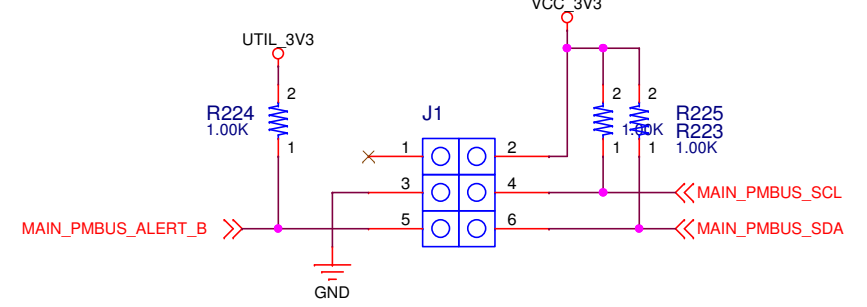
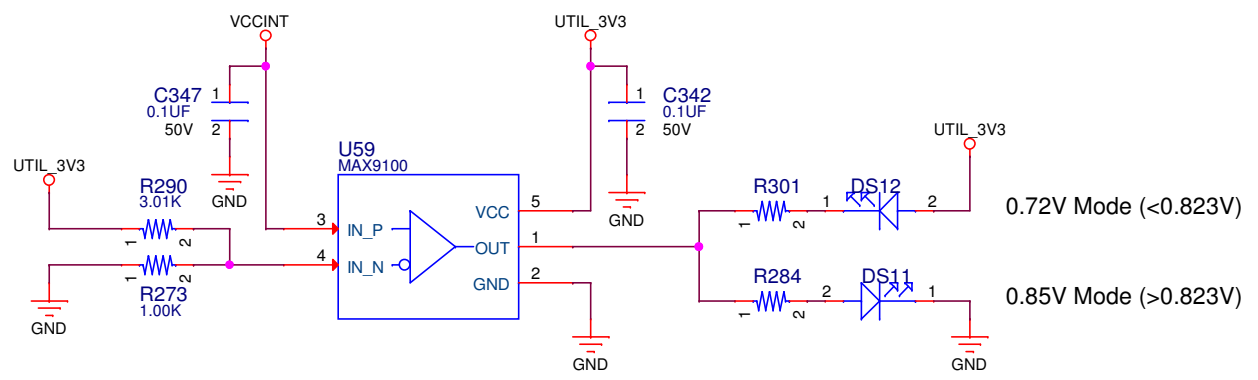


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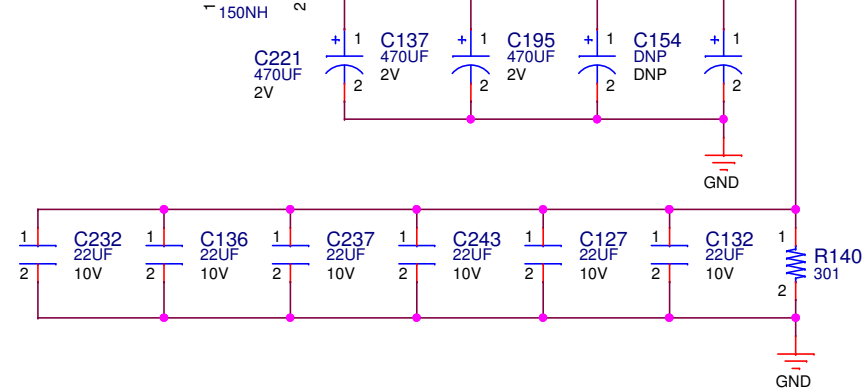
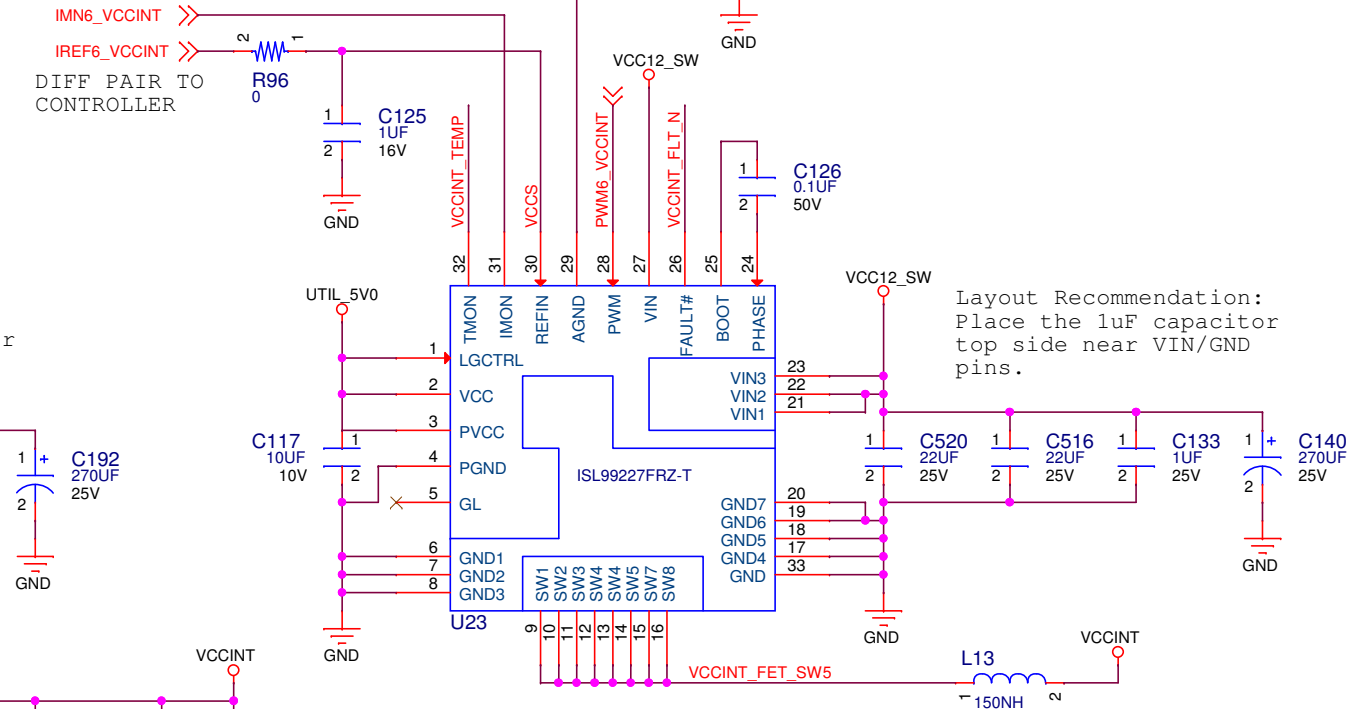
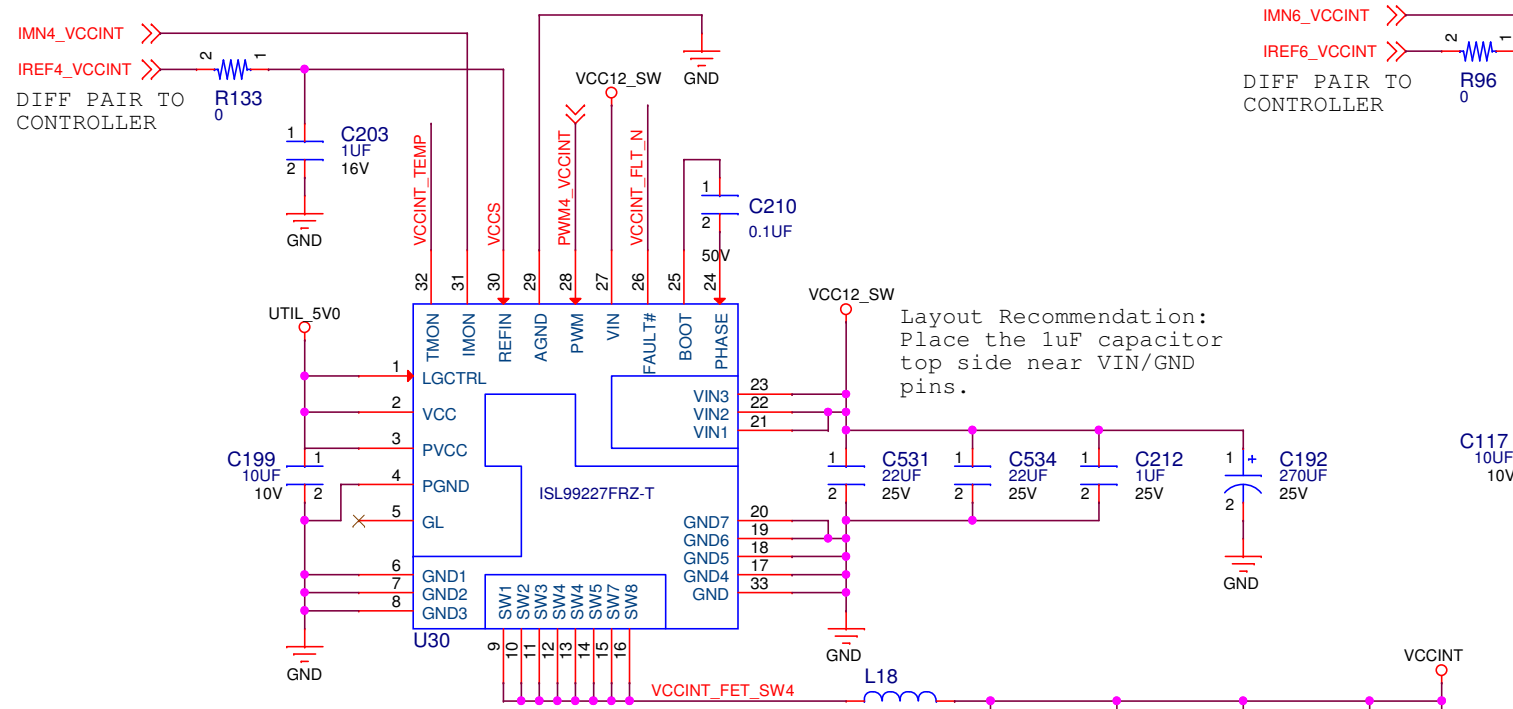
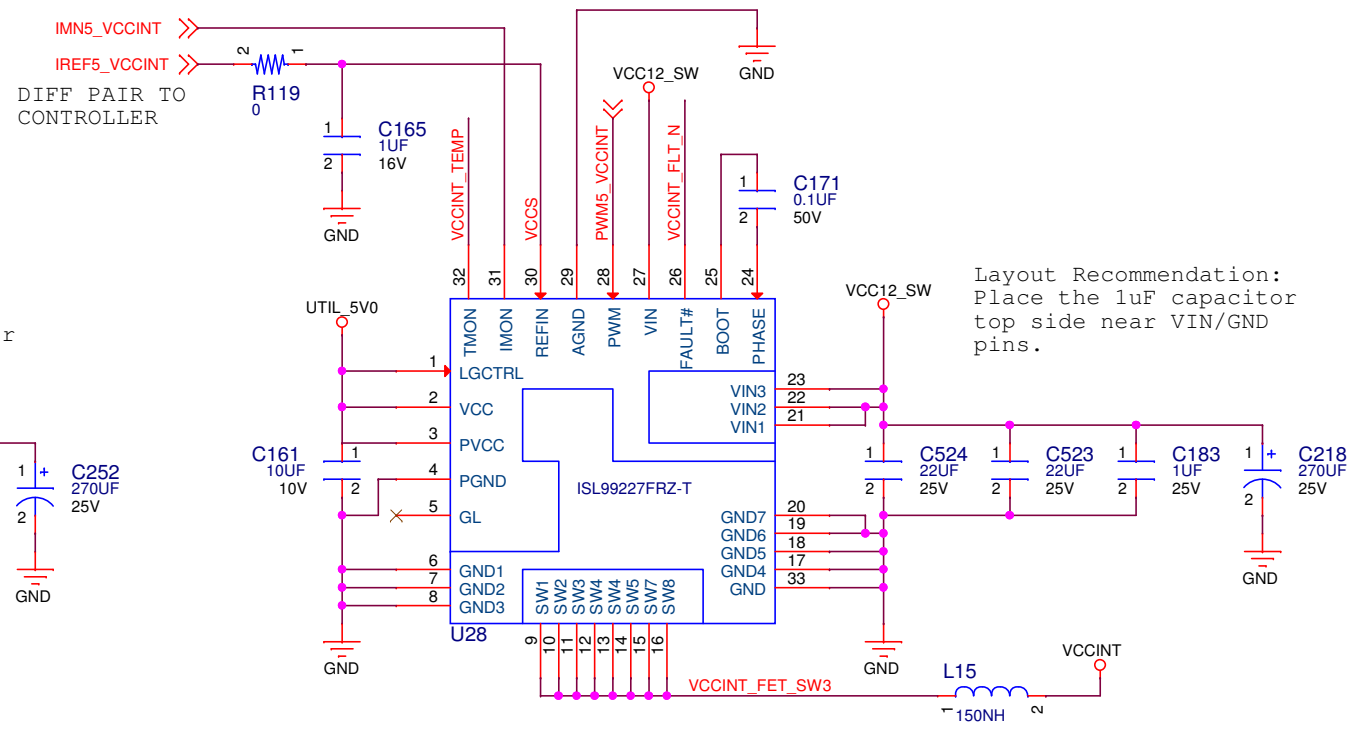
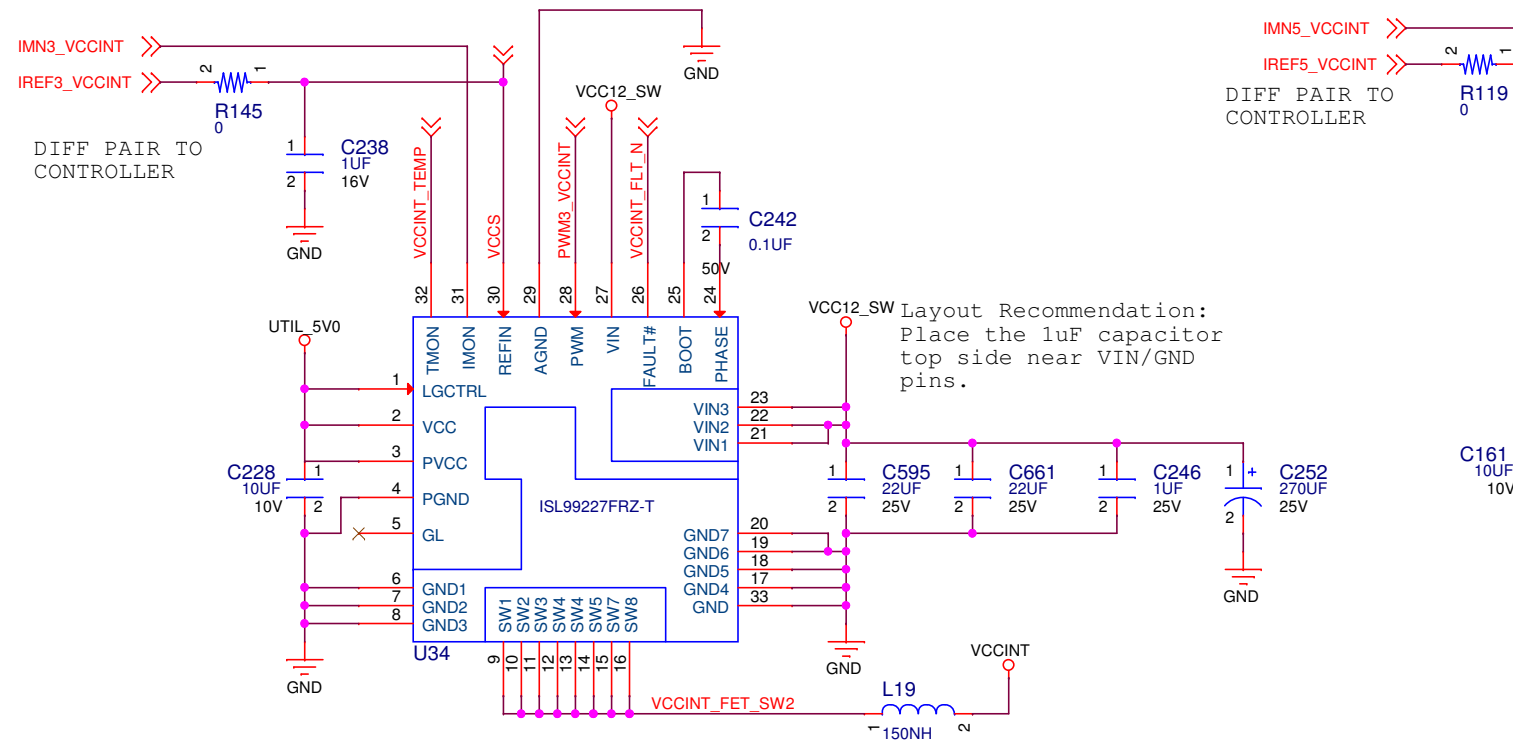


Layout Recommendation:
Place the 1uF capacitor
top side near VIN/GND
pins.

Layout Recommendation:
Place the 1uF capacitor
top side near VIN/GND
pins.

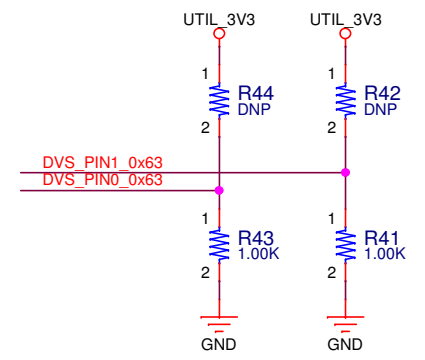
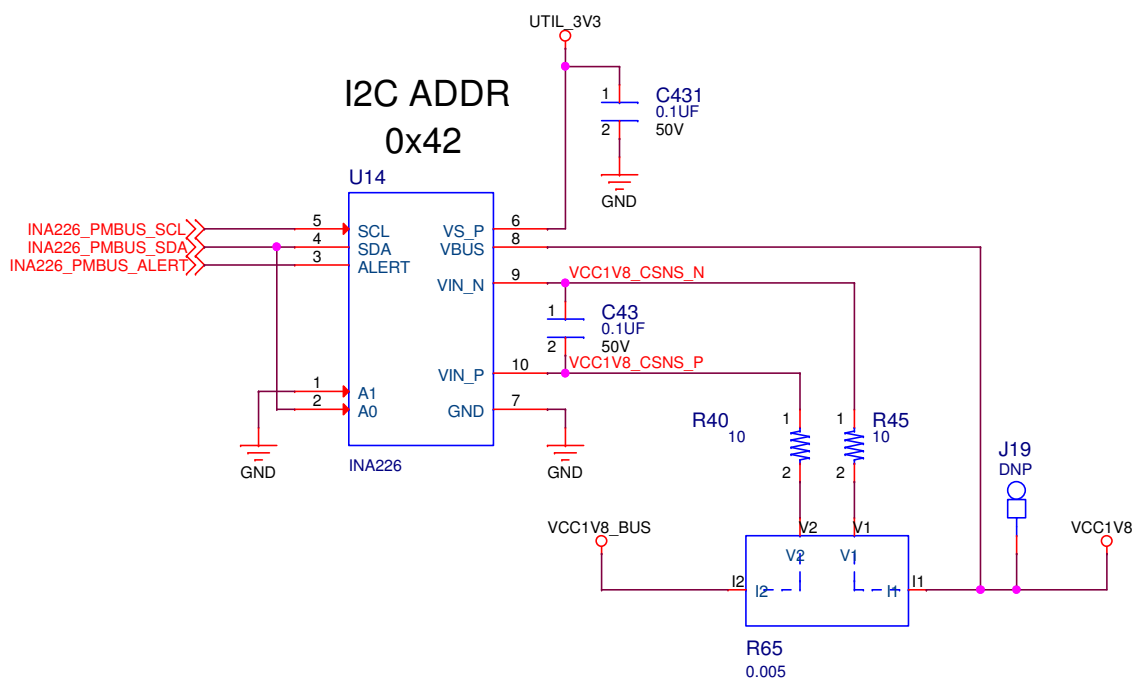
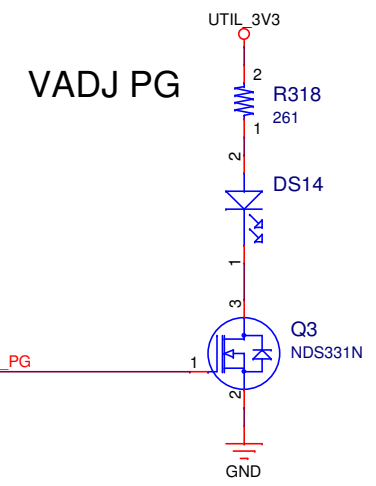
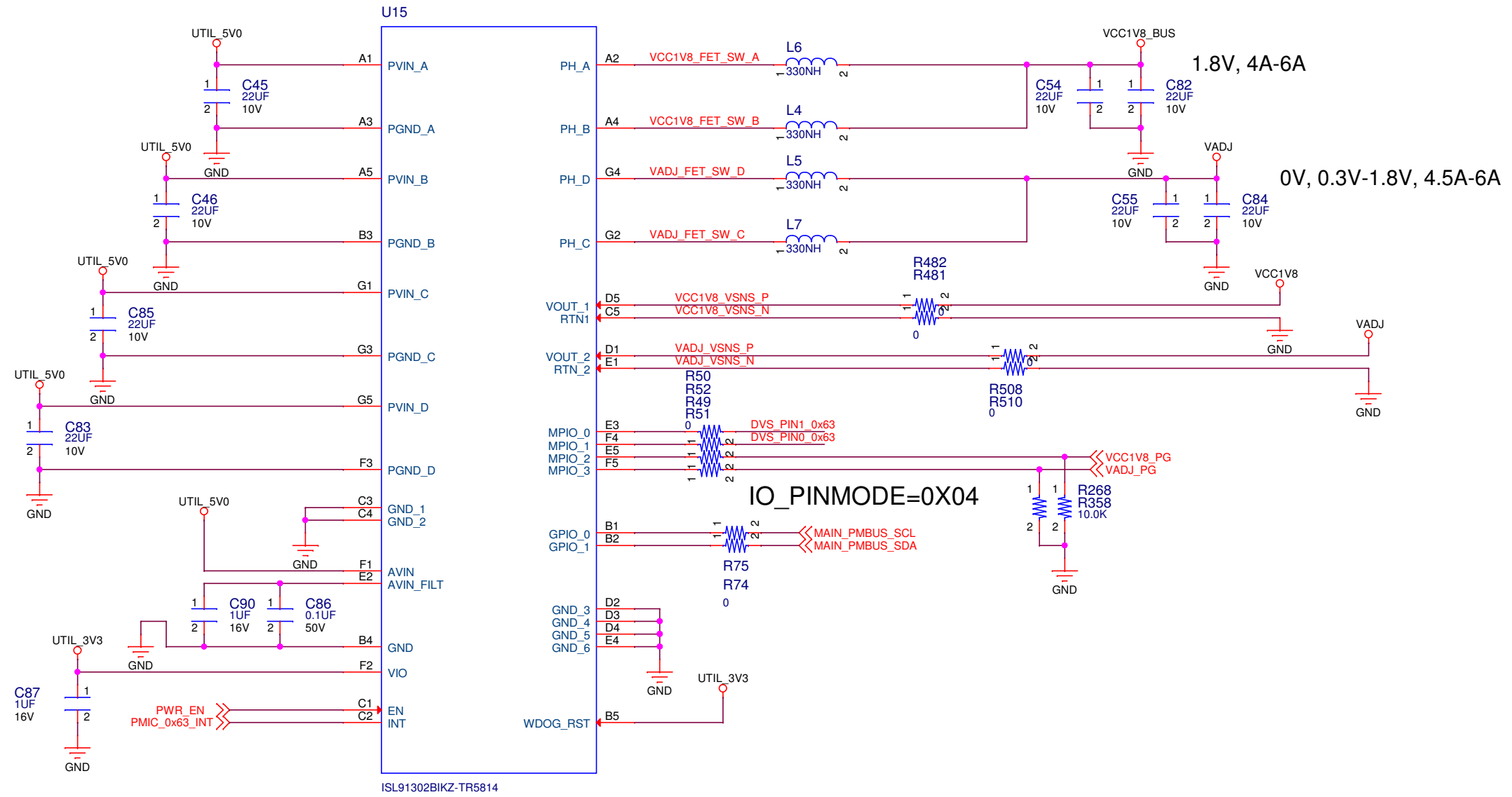


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Title: HW-U1-VCU128 054 VCCINT / VCCBRAM 1			
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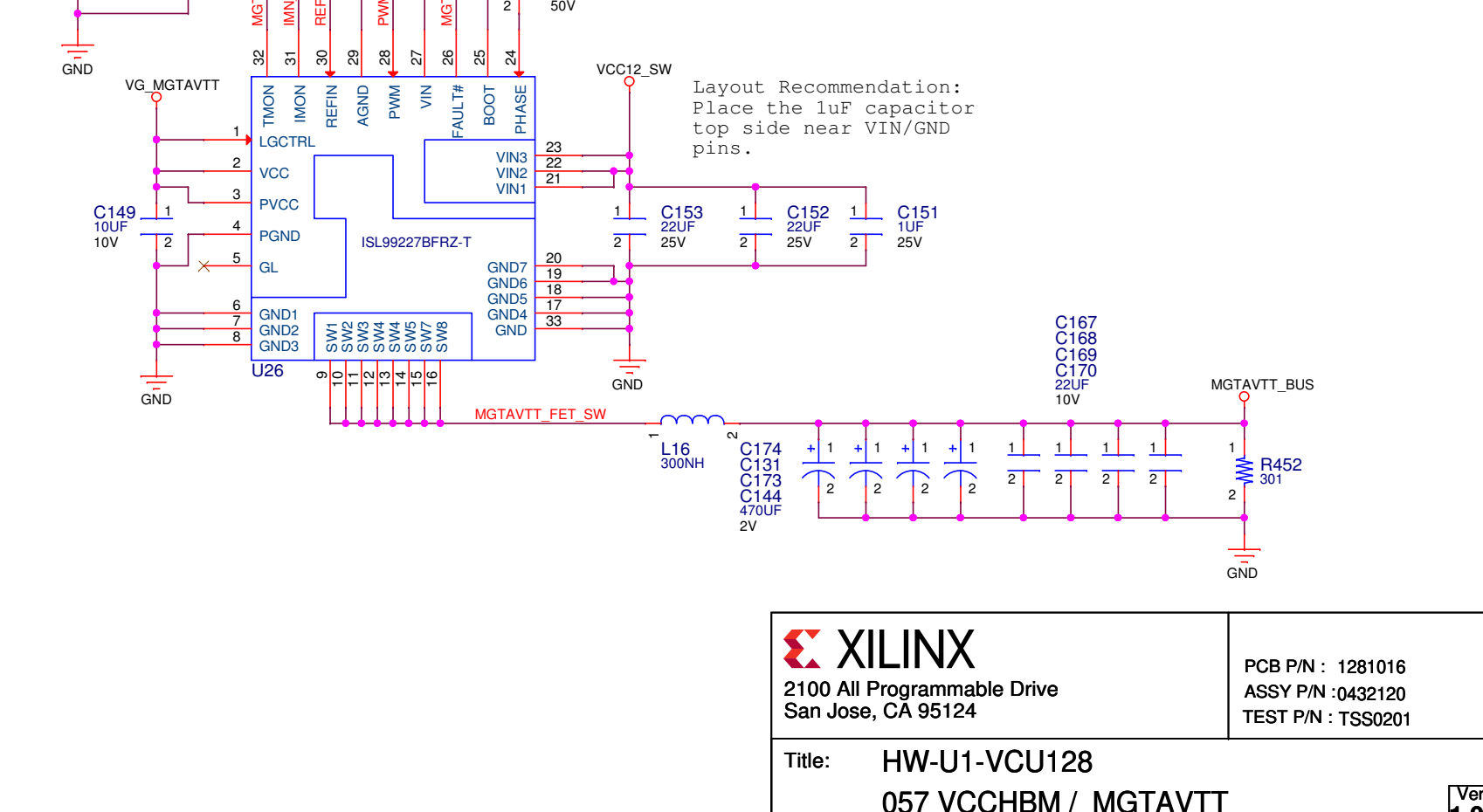
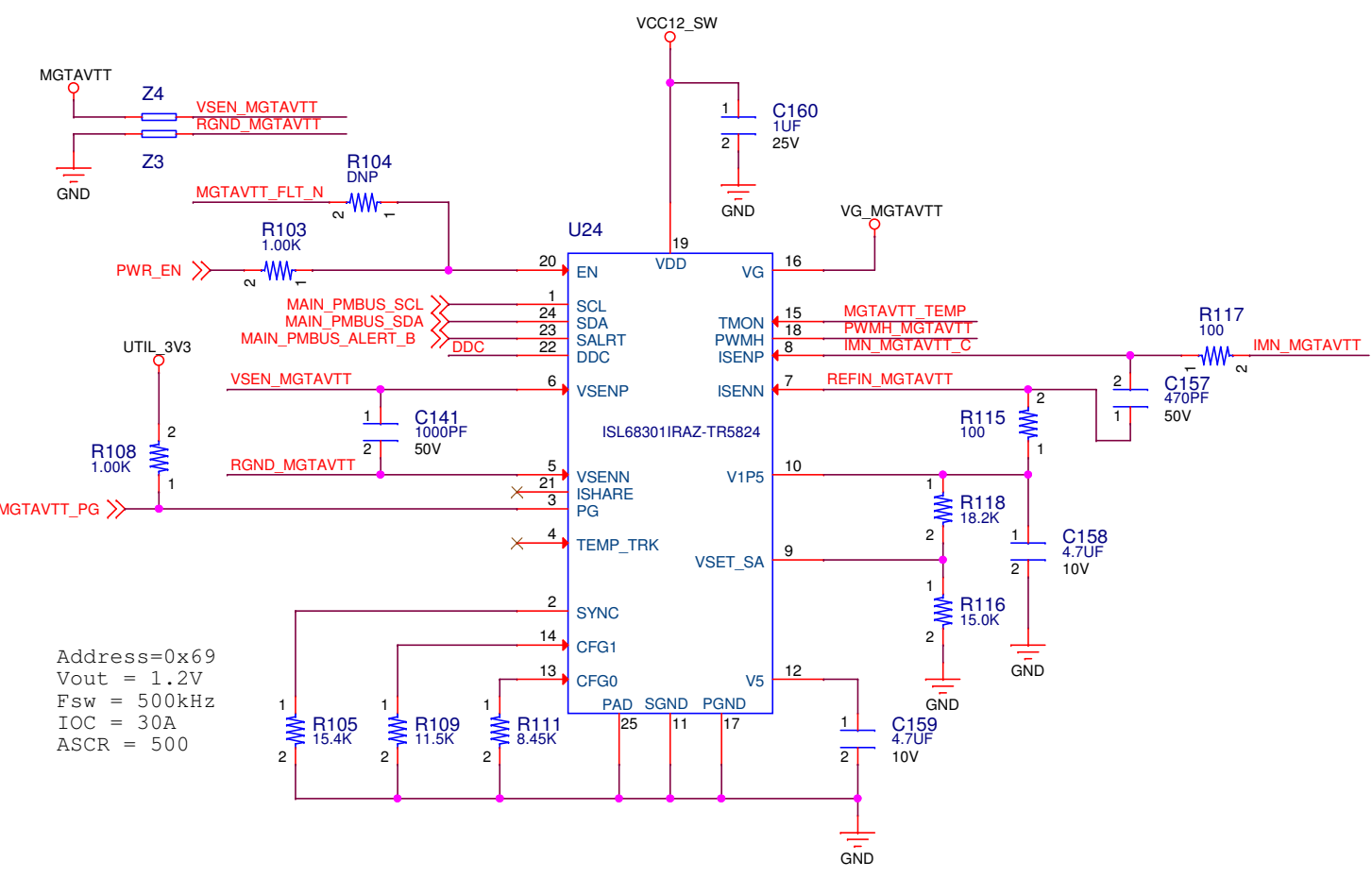
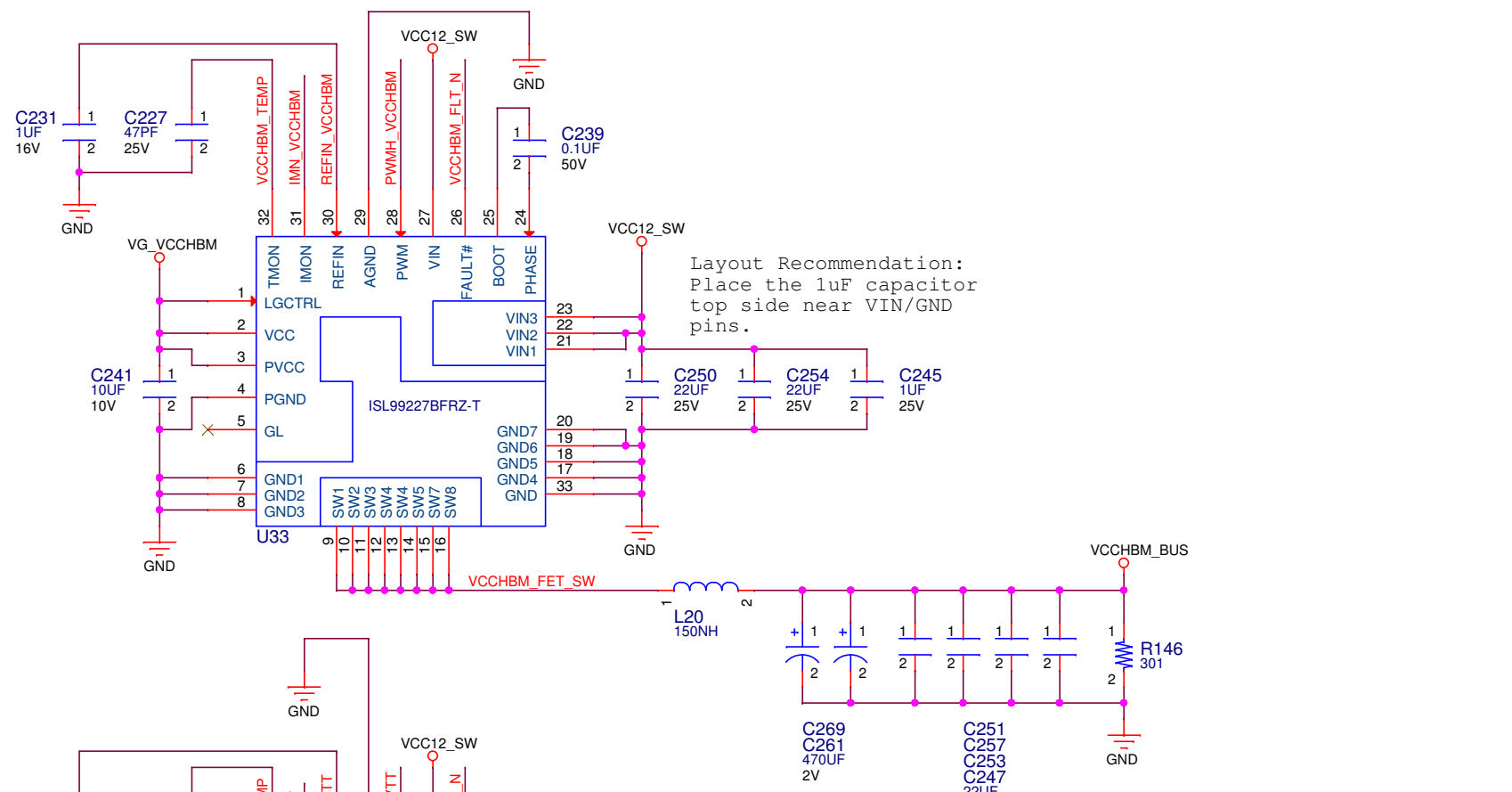
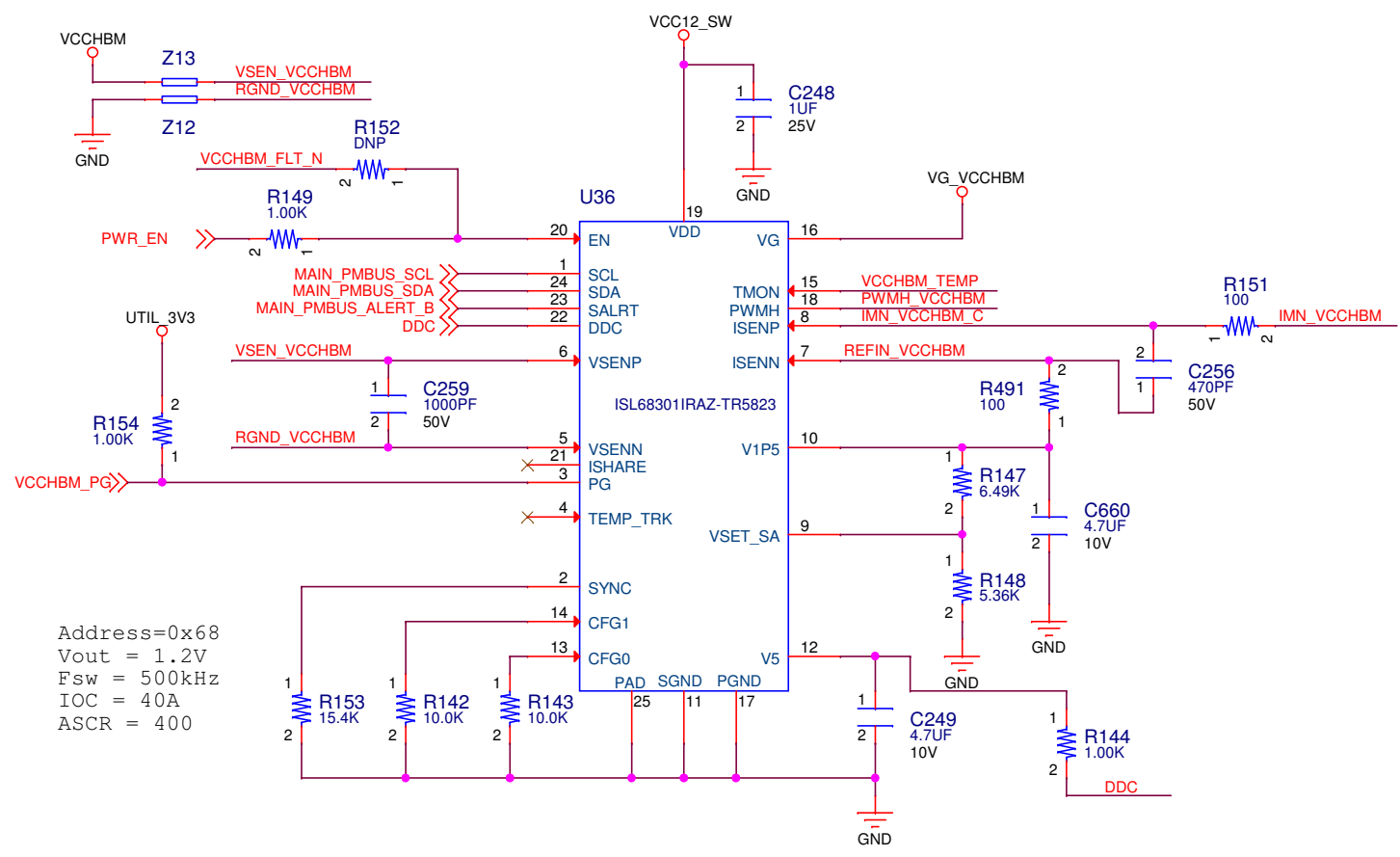


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Title: HW-U1-VCU128 055 VCCINT / VCCBRAM 2			
Size B	Date Modified: Wednesday, October 10, 2018	Document Number: 0381852	Ver 1.0 Rev 01
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PMBus Address = 0X63

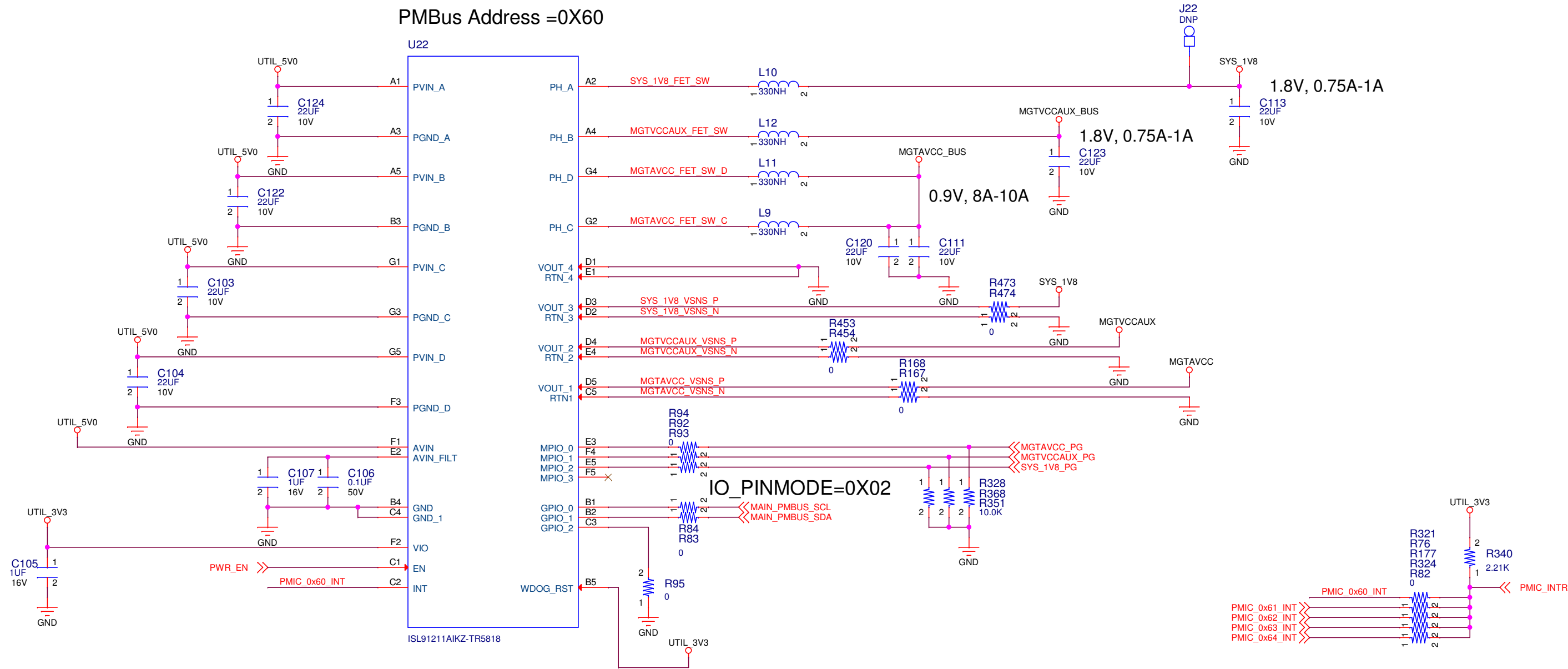


		PCB P/N : 1281016 ASSY P/N : 0432120 TEST P/N : TSS0201	
Title: HW-U1-VCU128 056 VCC1V8 / VADJ PMIC			
Size B	Date Modified: Wednesday, October 10, 2018	Document Number: 0381852	Ver 1.0 Rev 01
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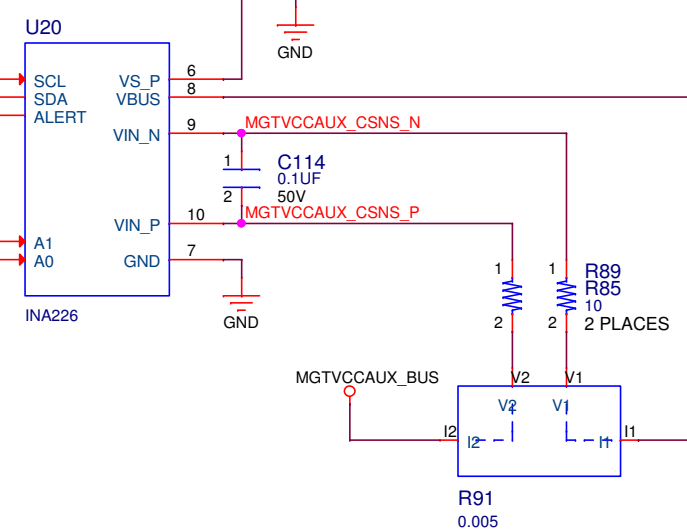


		PCB P/N : 1281016 ASSY P/N : 0432120 TEST P/N : TSS0201	
Title: HW-U1-VCU128 057 VCCHBM / MGTAVTT			
Size B	Date Modified: Wednesday, October 10, 2018	Document Number: 0381852	Ver 1.0 Rev 01
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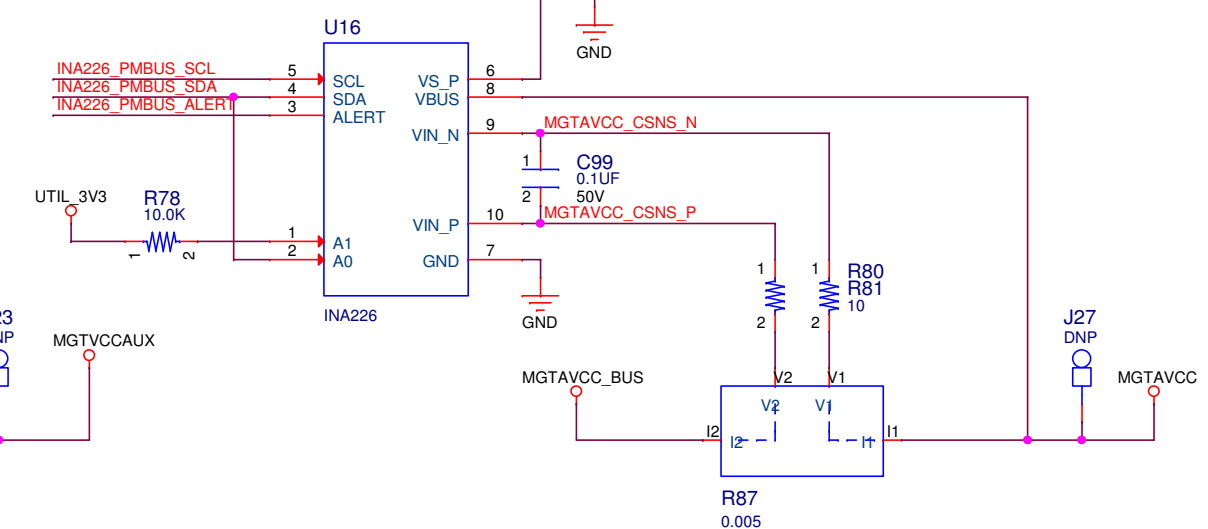
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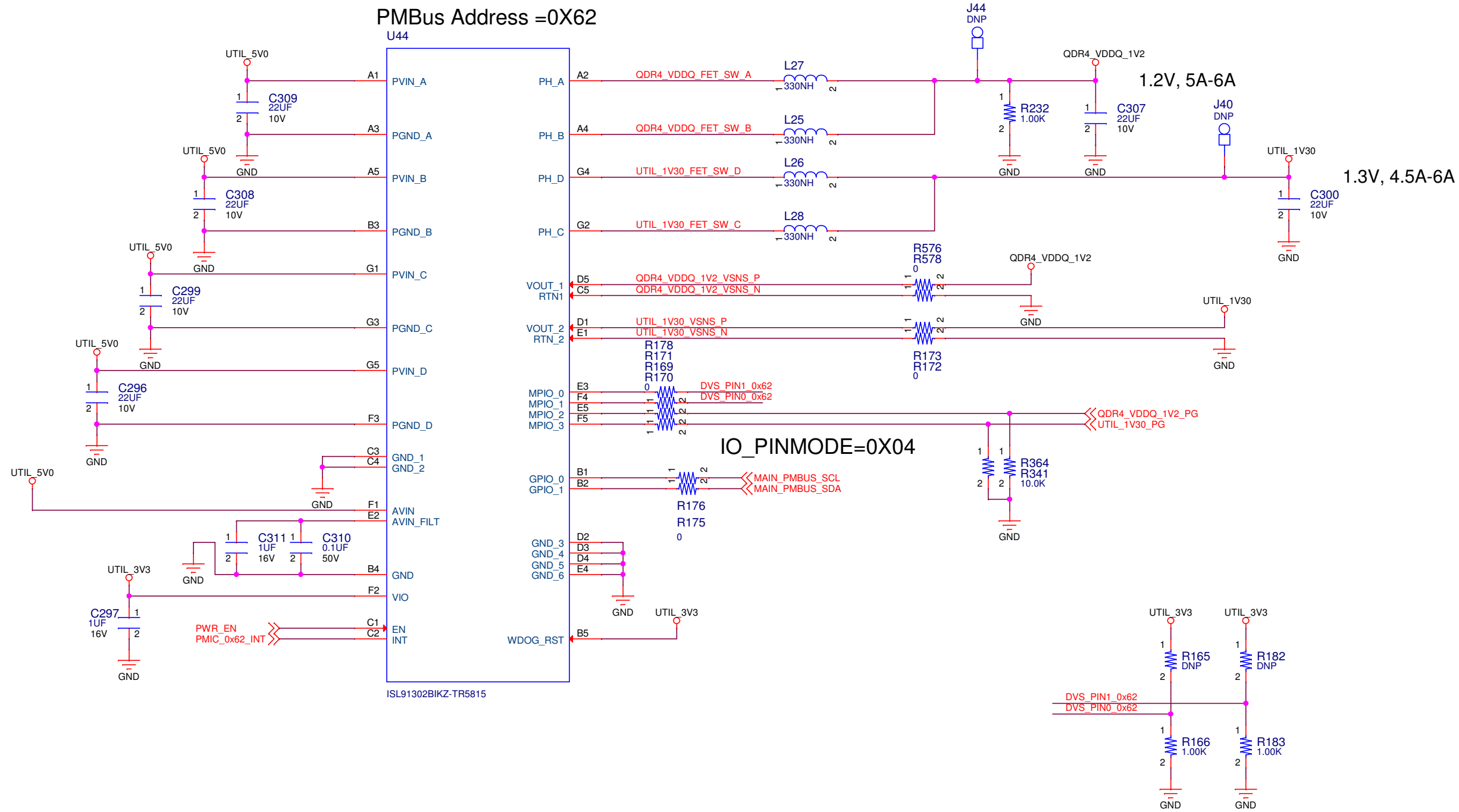
I2C ADDR 0x48



I2C ADDR 0x46

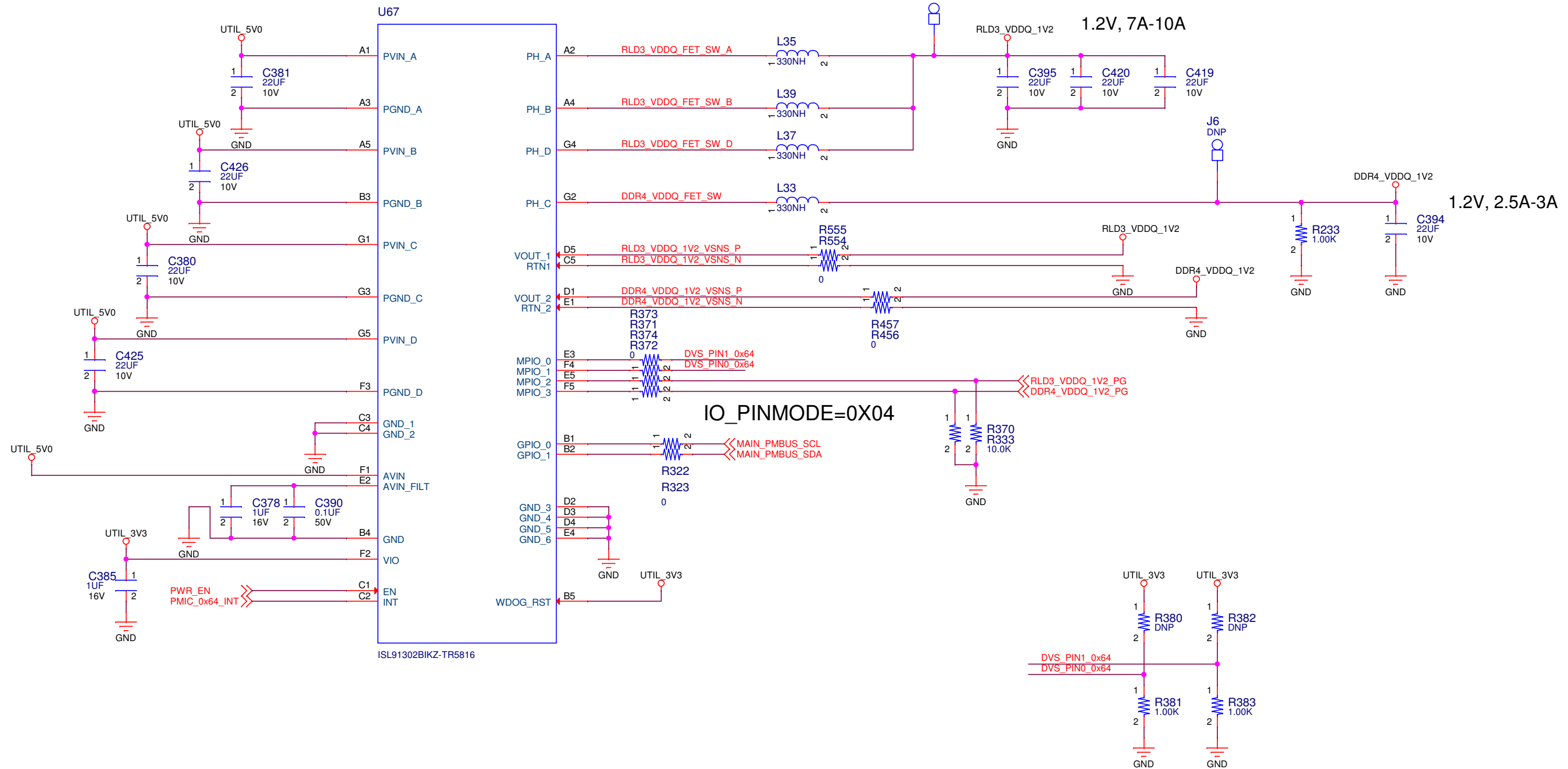


		PCB P/N : 1281016 ASSY P/N : 0432120 TEST P/N : TSS0201	
Title: HW-U1-VCU128 058 SYS_1V8 / MGTVCCAUX/AVCC			
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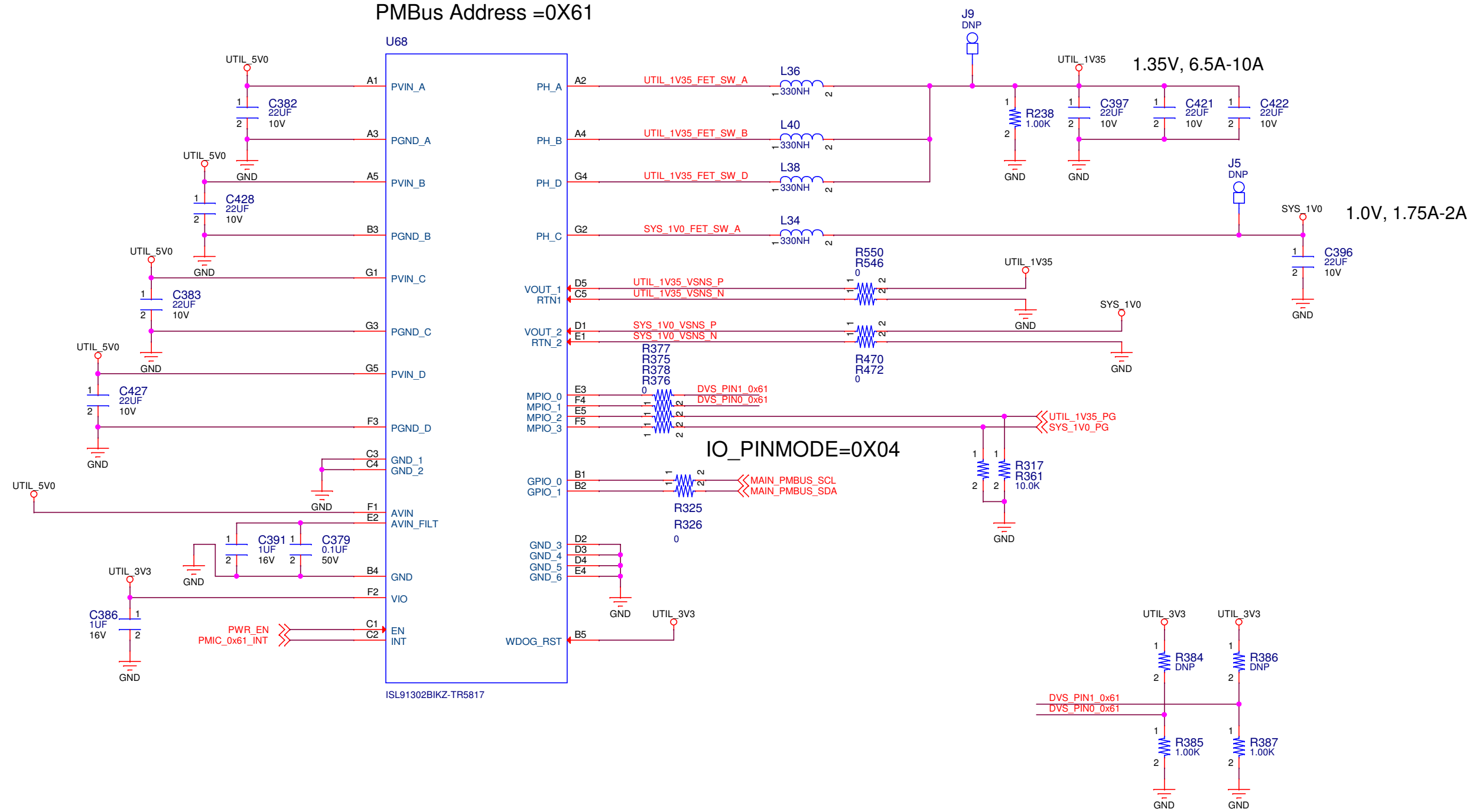
		PCB P/N : 1281016 ASSY P/N : 0432120 TEST P/N : TSS0201	
Title: HW-U1-VCU128 059 QDR4_VDDQ / UTIL_1V30 PMIC			
Size B	Date Modified: Wednesday, October 10, 2018	Document Number: 0381852	Ver 1.0 Rev 01
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PMBus Address =0X64

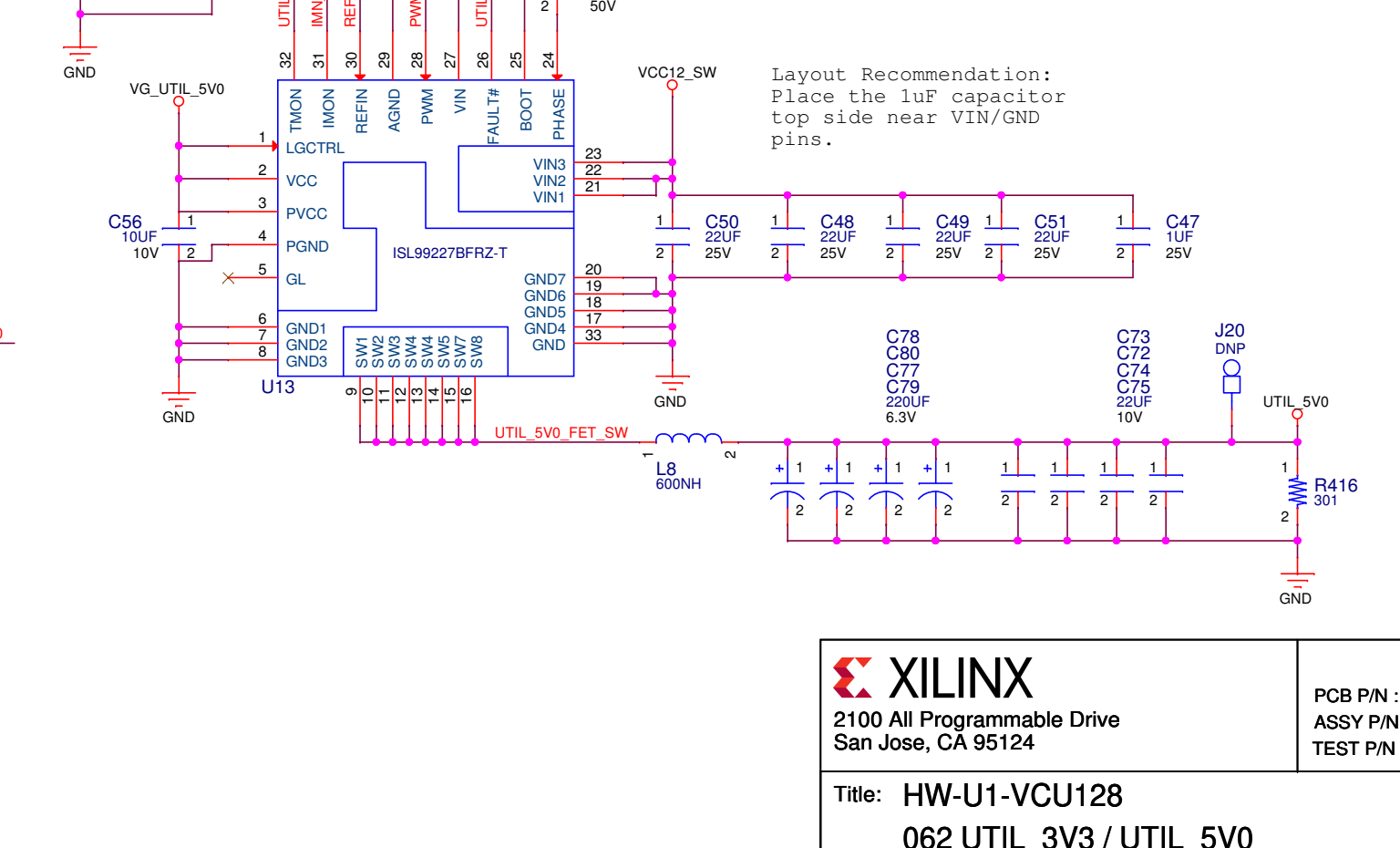
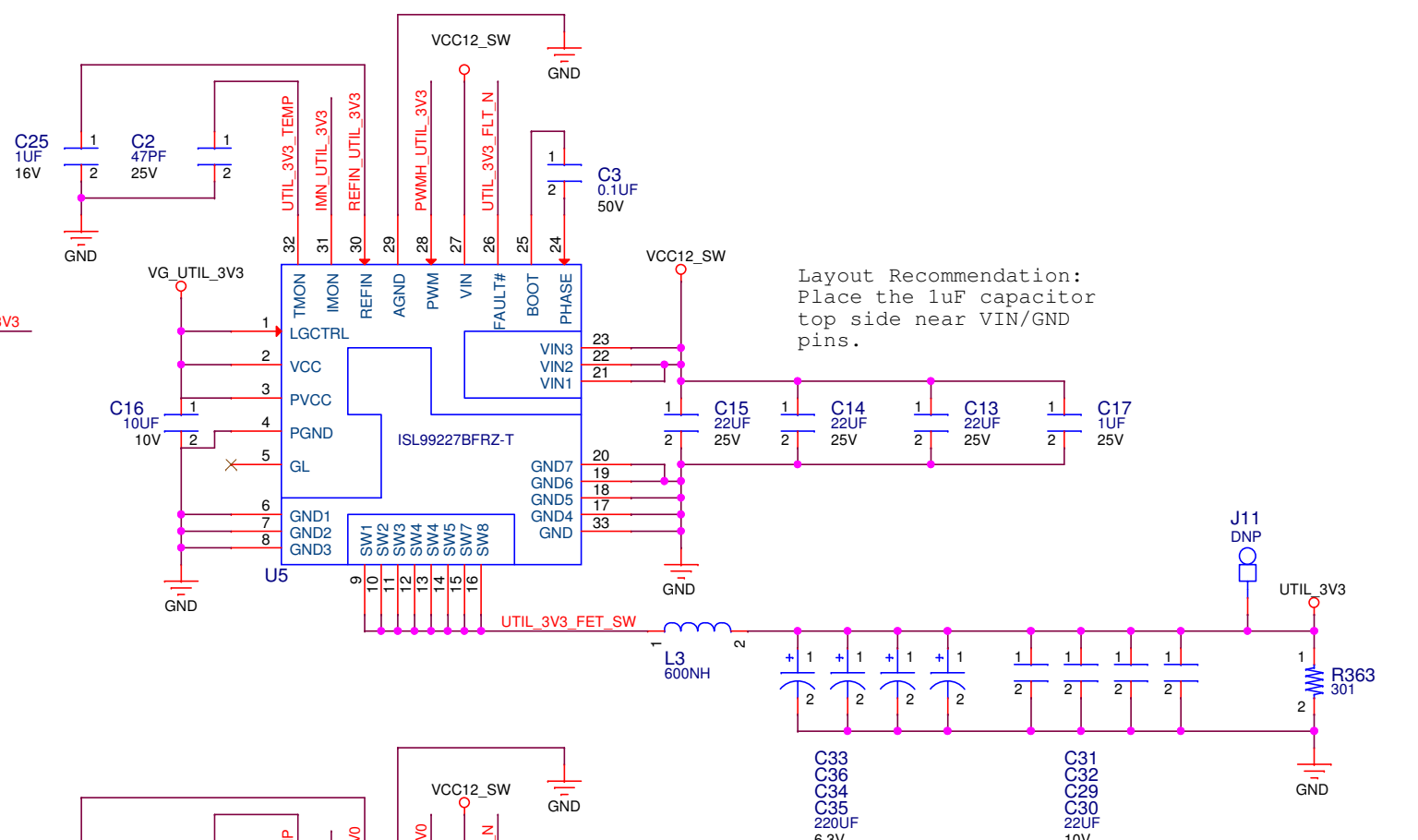
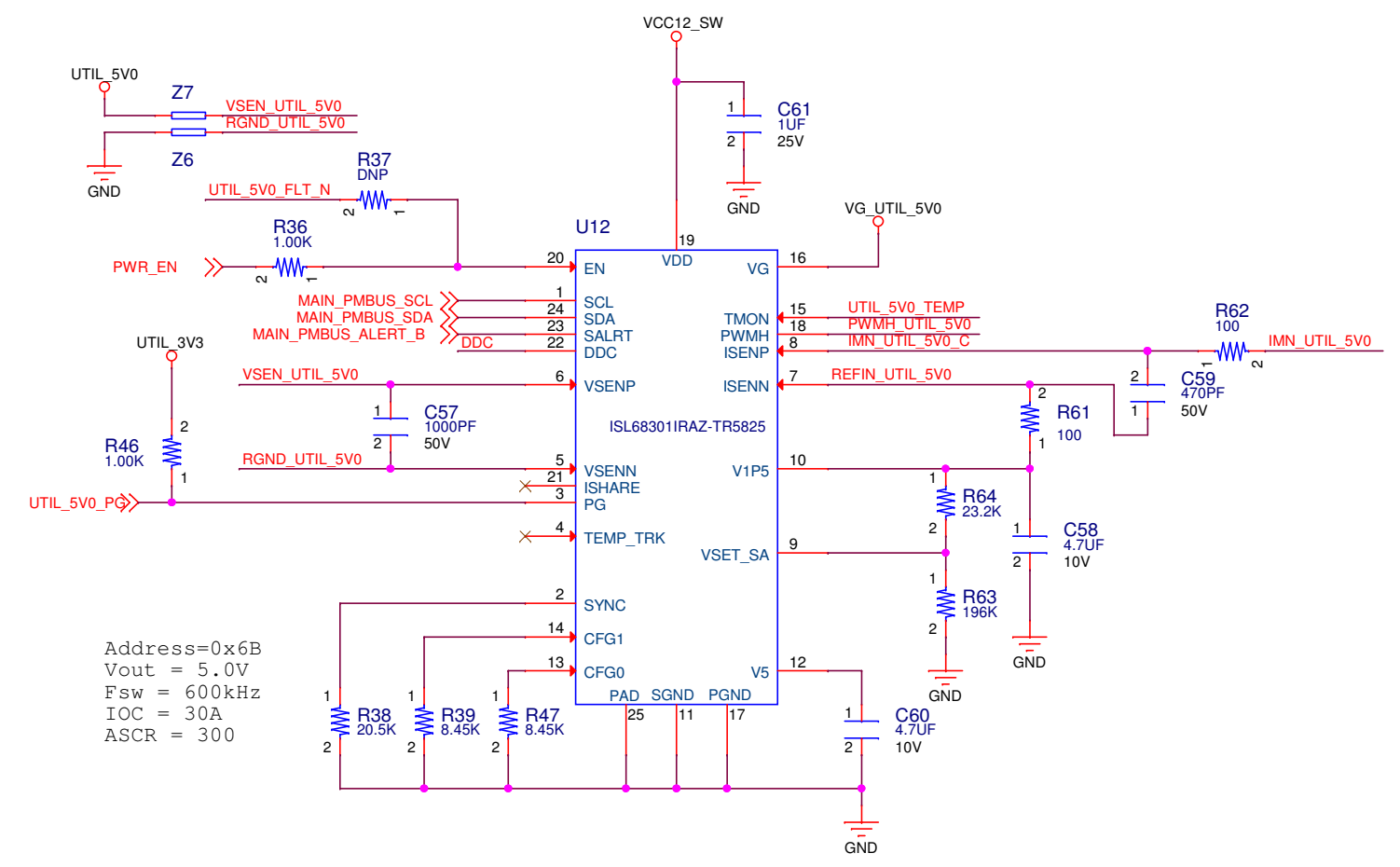
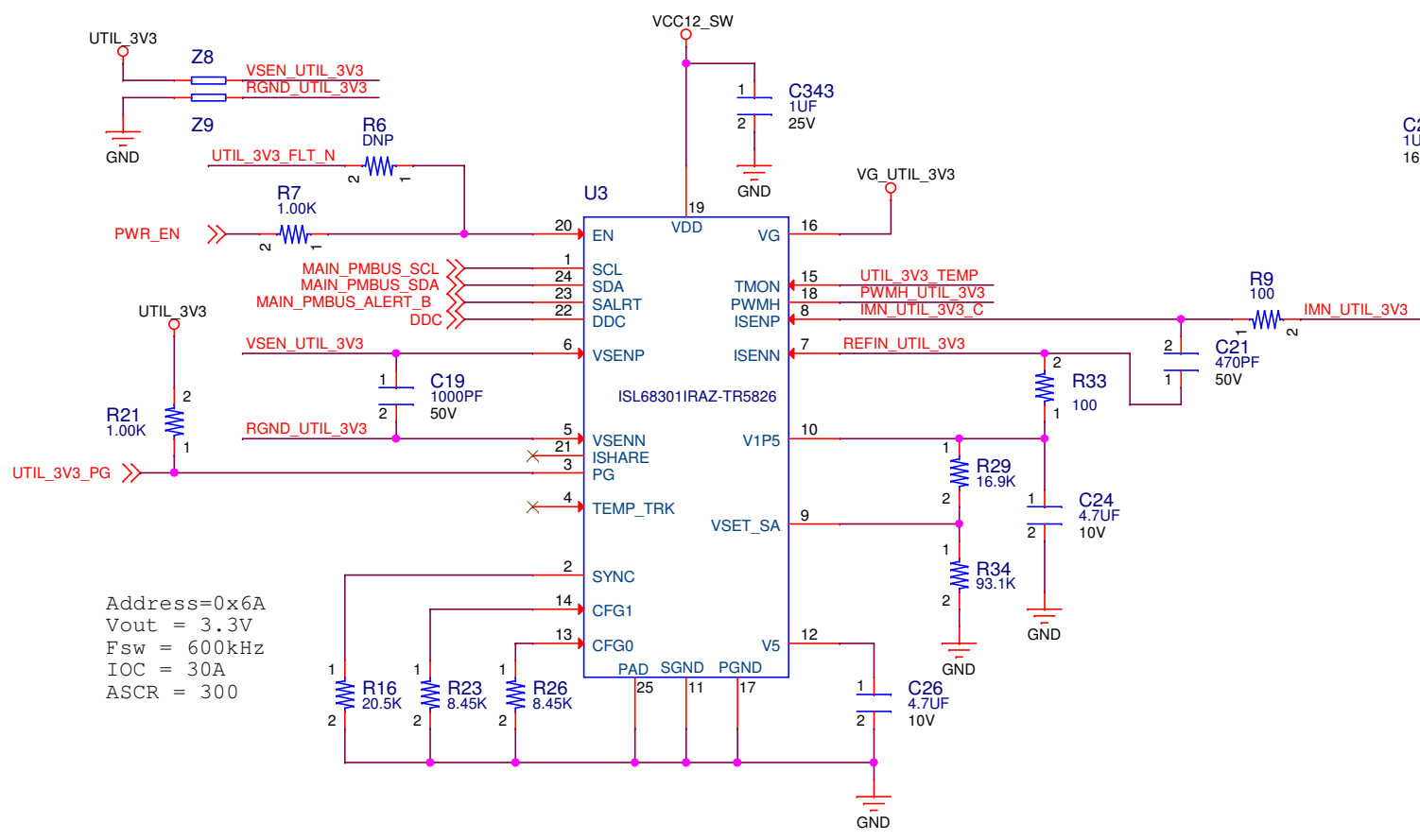


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Title: HW-U1-VCU128 060 DDR4_VDDQ / RLD3_VDDQ PMIC			
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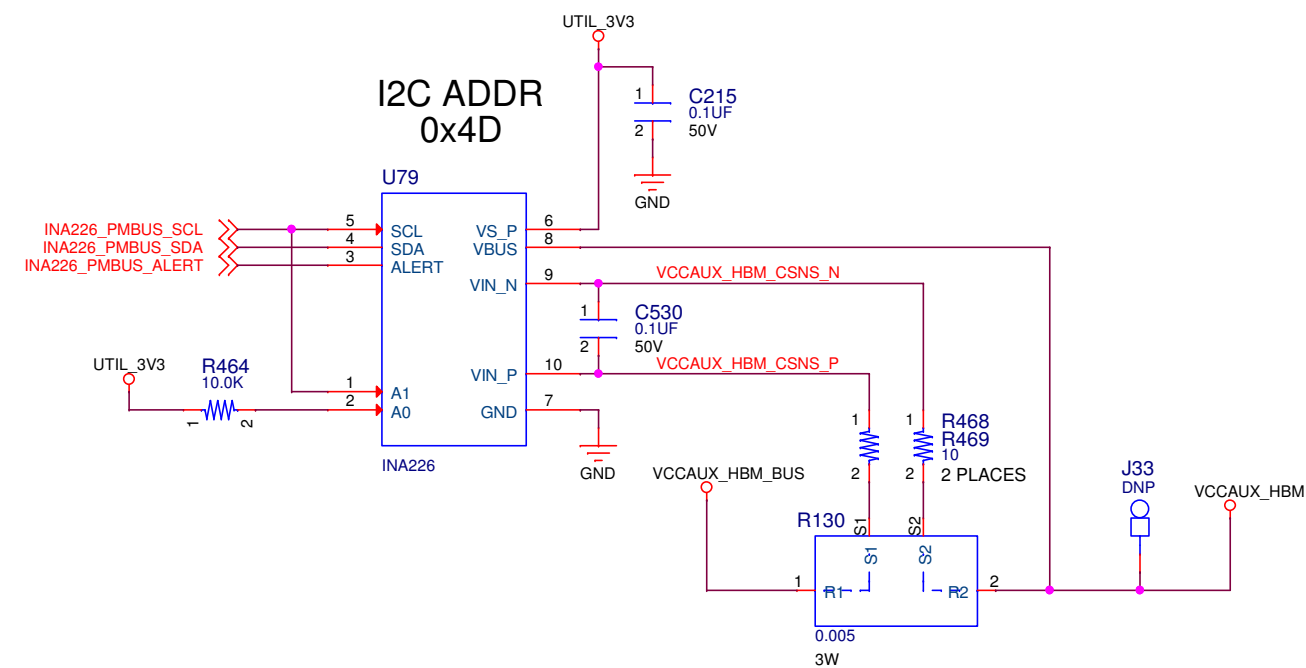
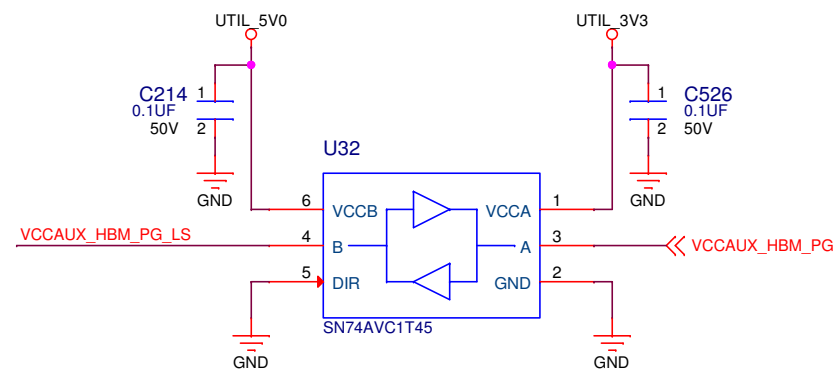
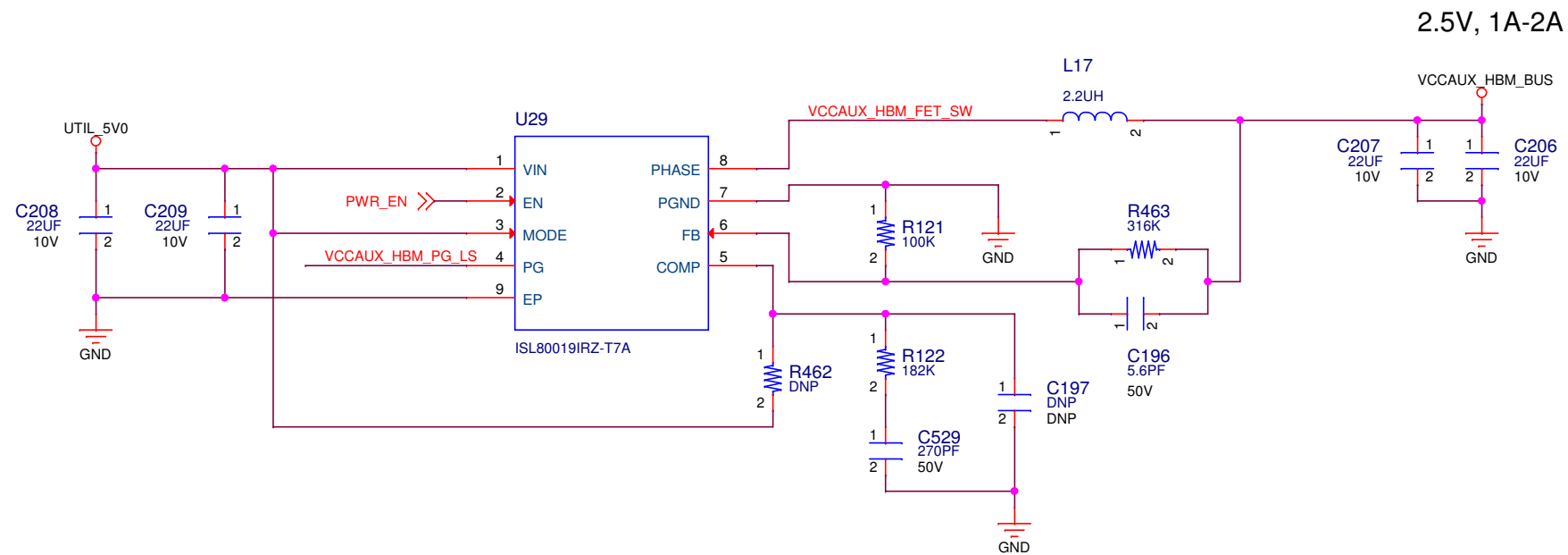
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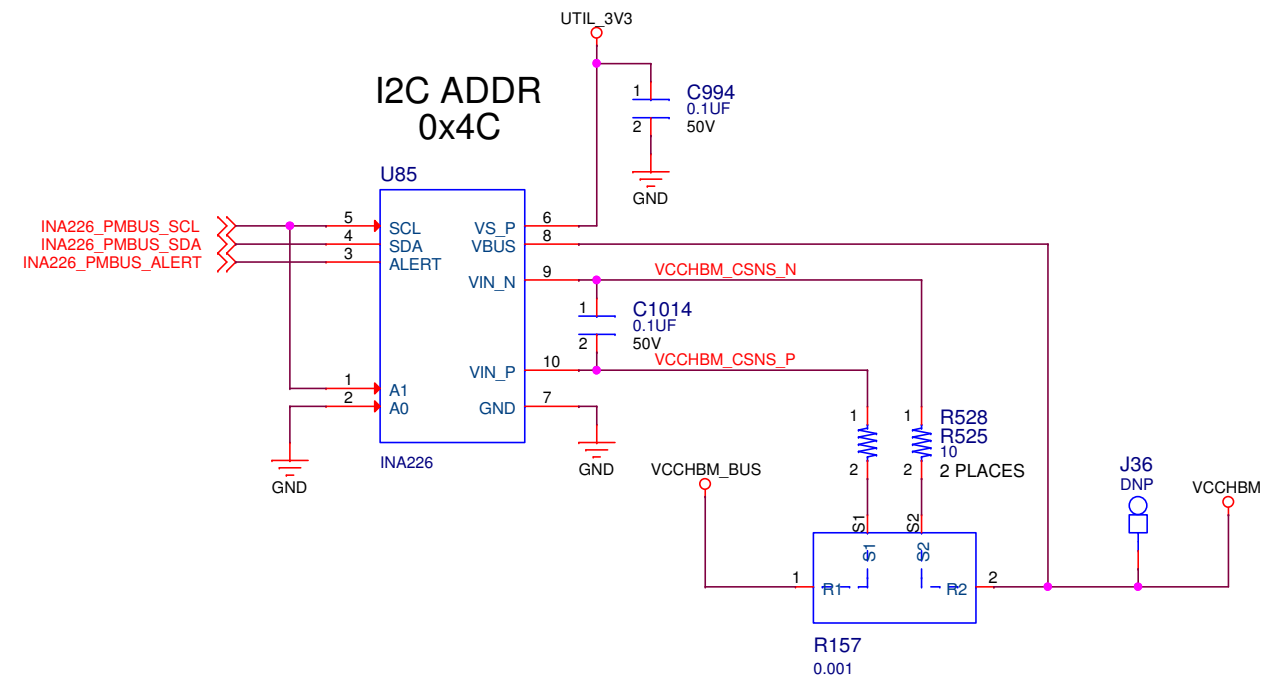
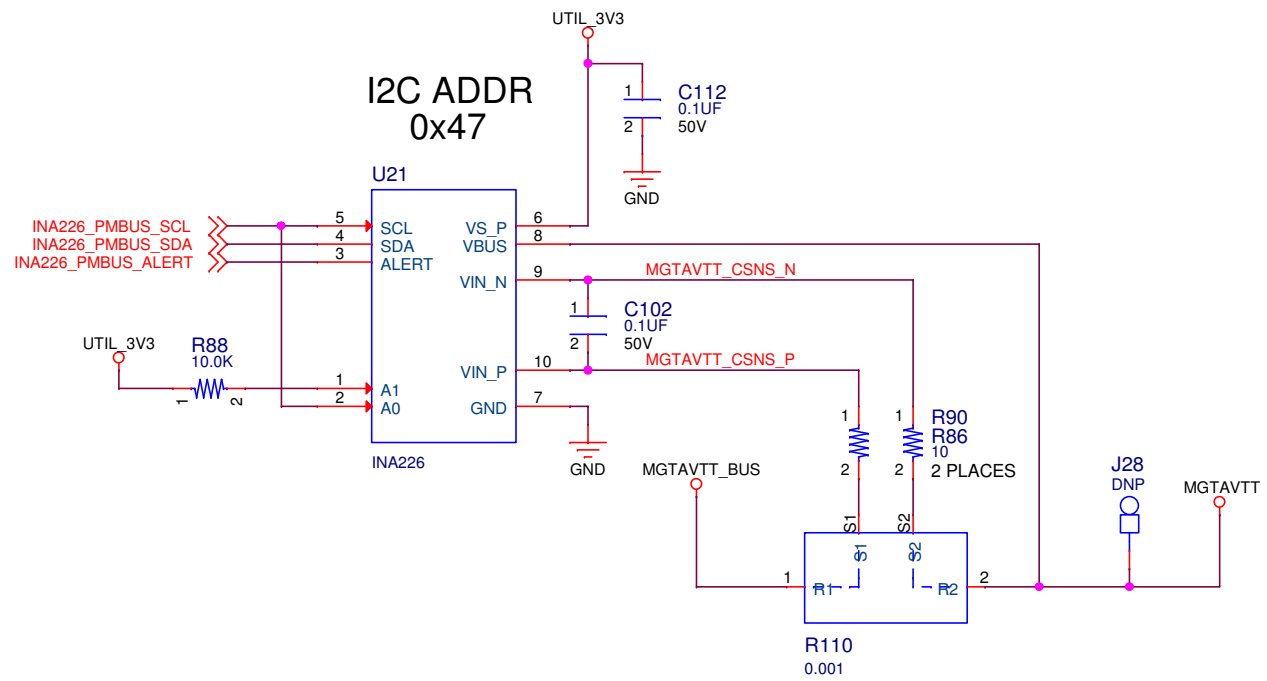
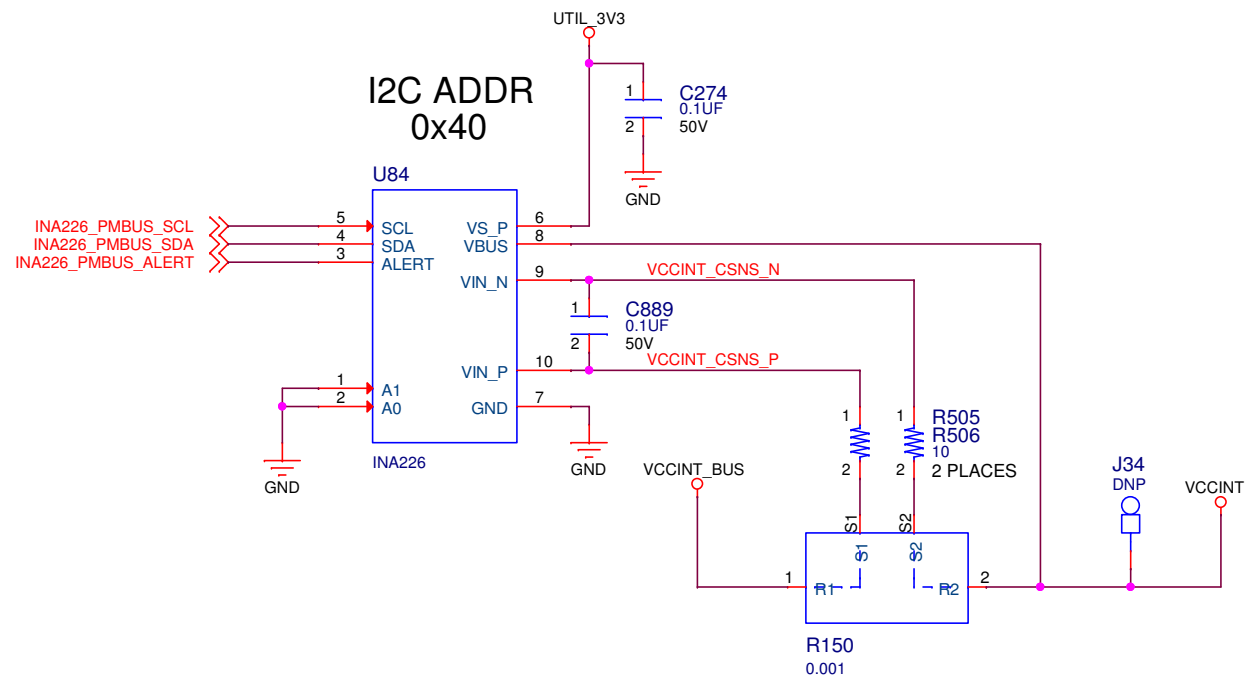
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Title: HW-U1-VCU128 061 UTIL_1V35 / SYS_1V0 PMIC			
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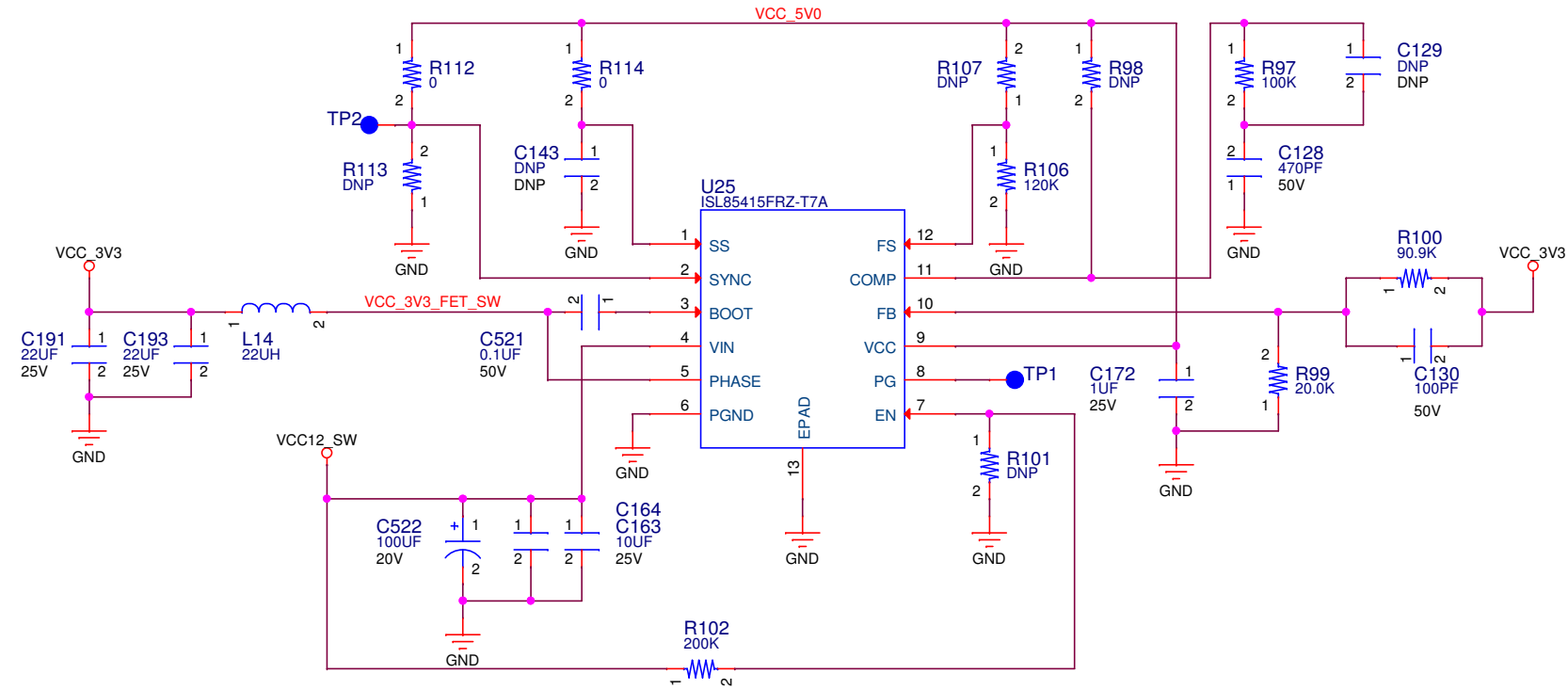
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Title: HW-U1-VCU128 062 UTIL_3V3 / UTIL_5V0			
Size B	Date Modified: Wednesday, October 10, 2018	Document Number: 0381852	Ver 1.0 Rev 01
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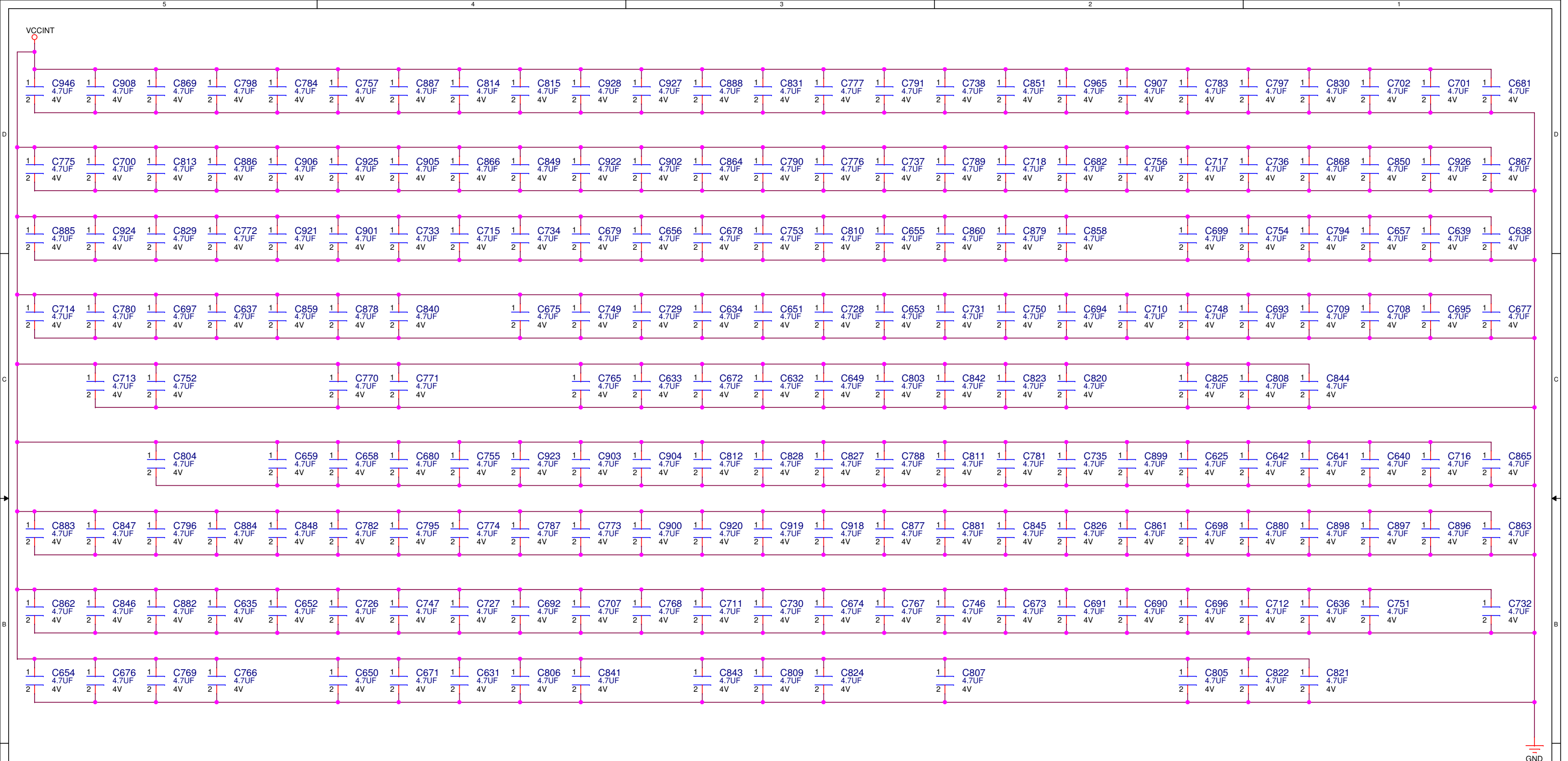
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Title: HW-U1-VCU128 063 VCCAUX_HBM			
Size B	Date Modified: Wednesday, October 10, 2018	Document Number: 0381852	Ver 1.0 Rev 01
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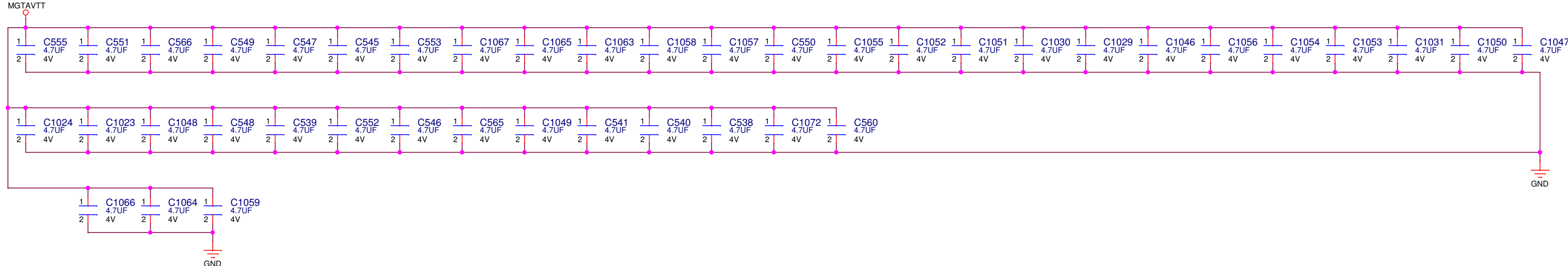
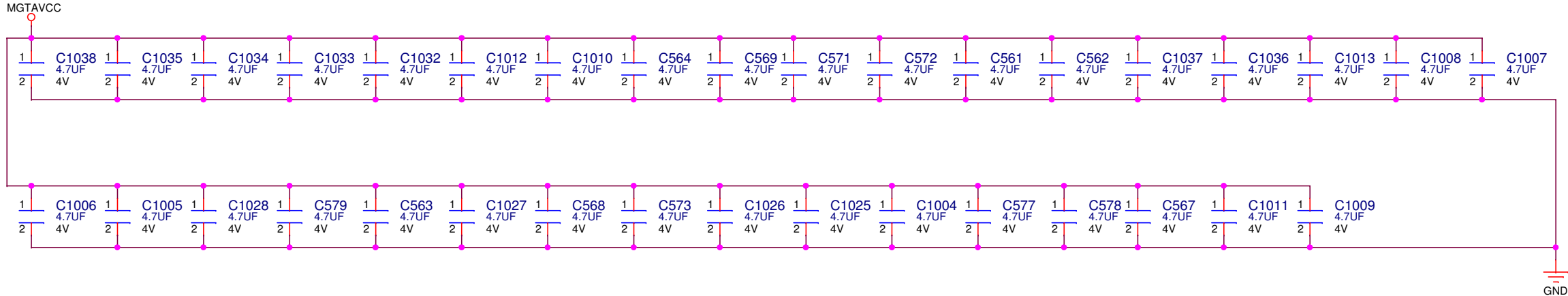
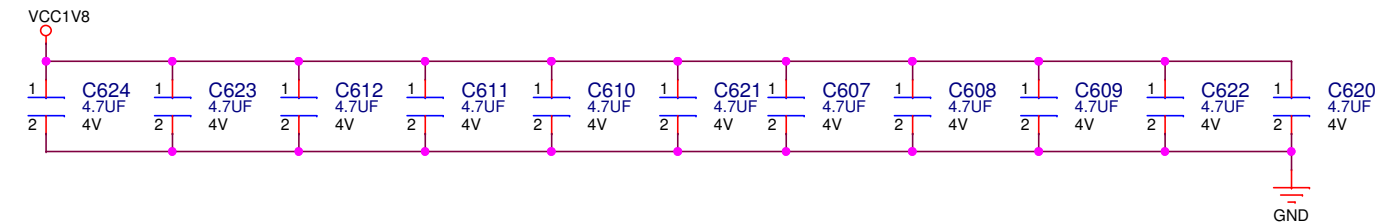
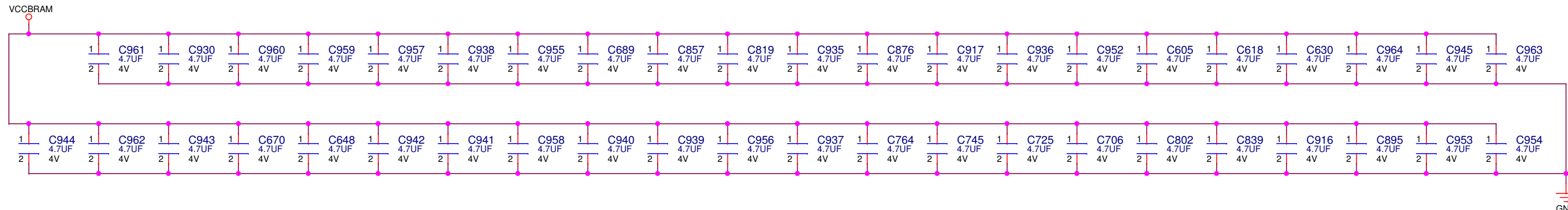
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Title: HW-U1-VCU128 064 INA226 Current Sense			
Size B	Date Modified: Wednesday, October 10, 2018	Document Number: 0381852	Ver 1.0 Rev 01
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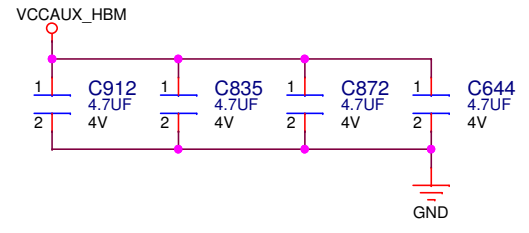
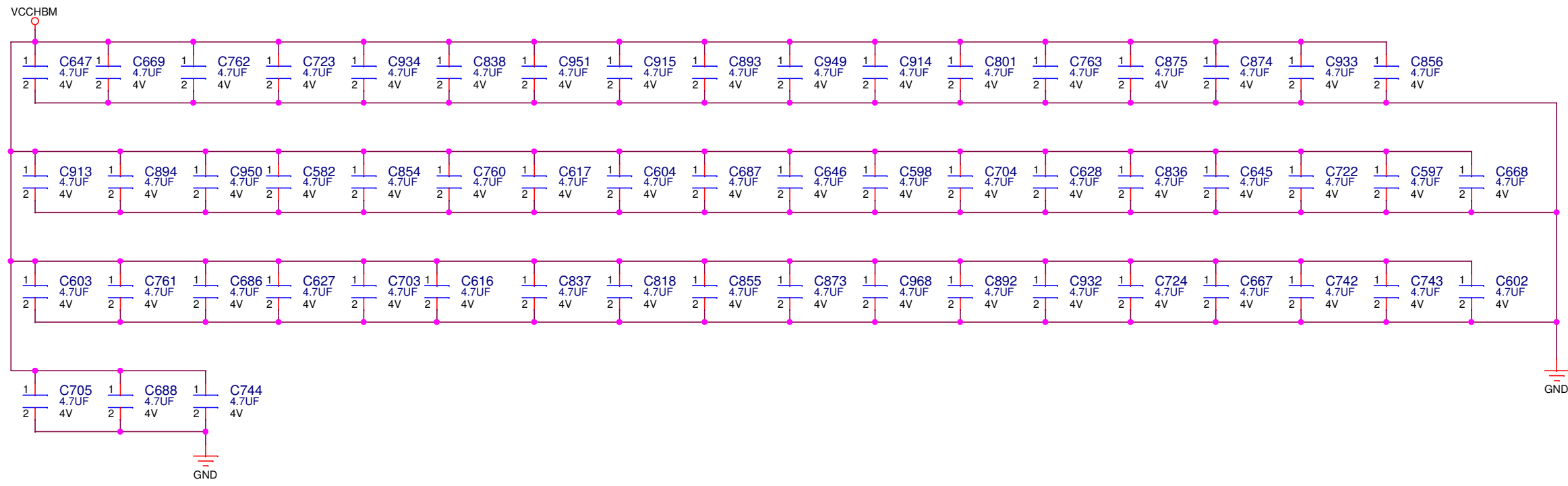
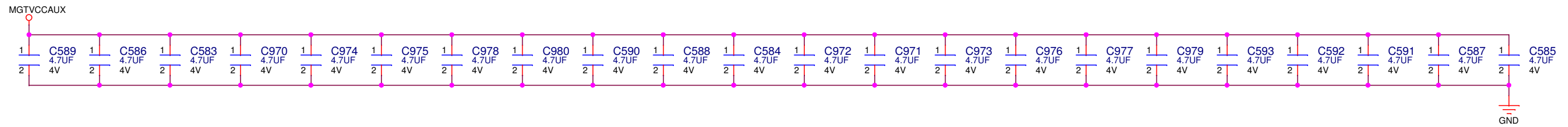
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Title: HW-U1-VCU128 065 VCC_3V3			
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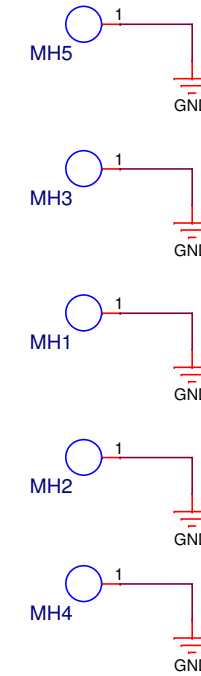
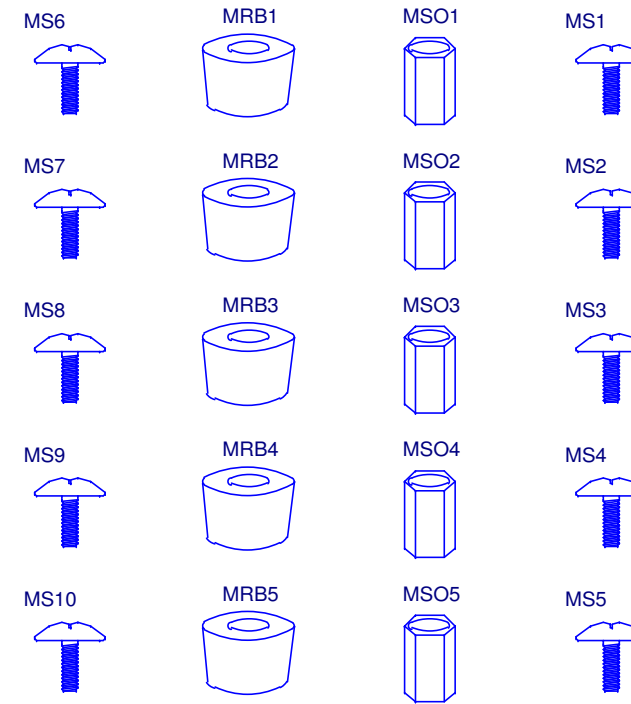
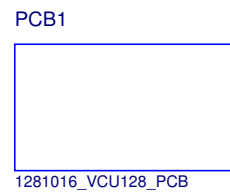
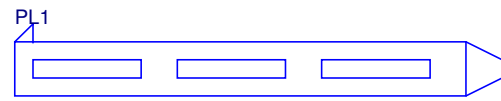
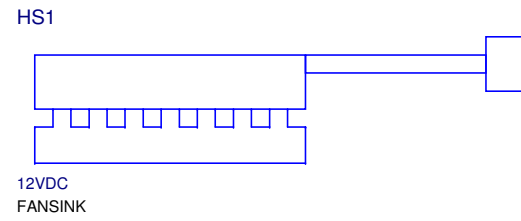
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Title: HW-U1-VCU128 066 Additional Decoupling Caps			
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		PCB P/N : 1281016 ASSY P/N : 0432120 TEST P/N : TSS0201	
Title: HW-U1-VCU128 067 Additional Decoupling Caps			
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		PCB P/N : 1281016 ASSY P/N : 0432120 TEST P/N : TSS0201	
Title: HW-U1-VCU128 068 Additional Decoupling Caps			
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		PCB P/N : 1281016 ASSY P/N : 0432120 TEST P/N : TSS0201	
Title: HW-U1-VCU128 069 Mechanicals			
Size B	Date Modified: Wednesday, October 10, 2018	Document Number: 0381852	Ver 1.0 Rev 01
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