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MediaTek Inc.		<small>No. 1, Daxing Rd. 1, Hsinchu Science Park Hsinchu, Taiwan 300, R.O.C.</small>		<small>TEL: +886-3-567-8788 Fax: +886-3-578-7819</small>
Change History				
	Title			
	Size	Document Number	Drawn	Rev
C		MT7986A RFB		V10
Date:	Monday, March 28, 2022	Sheet	1	of 14



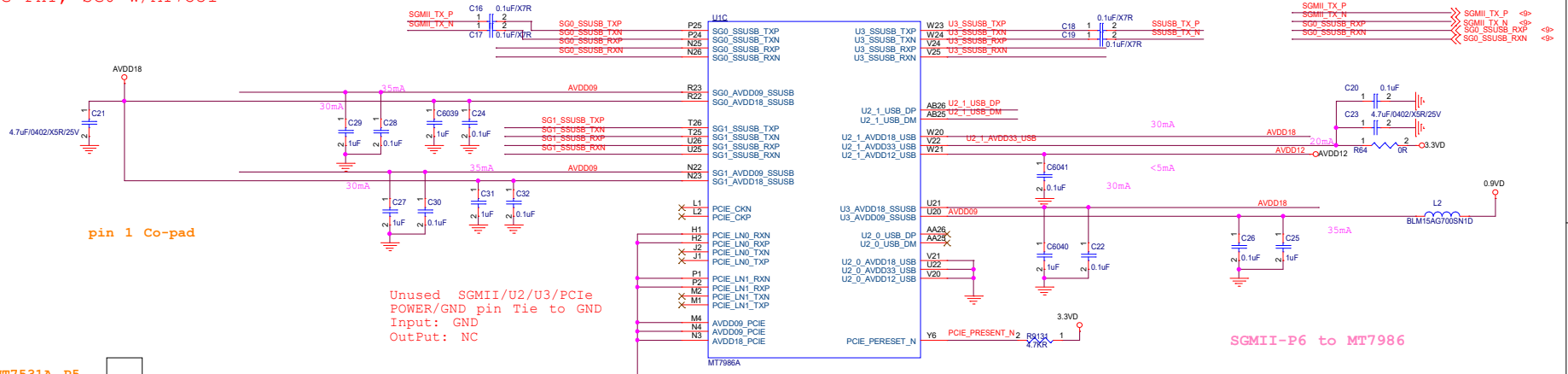
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Block Diagram & Power on sequence				
	Title			
	Size	Document Number	Drawn	Rev
C		MT7986A RFB		V10
Date:	Monday, March 28, 2022	Sheet	3	of 14

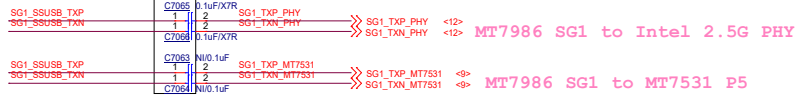
1. U2_1 w/ U3
2. SG1 w/ 2.5G PHY, SG0 w/MT7531

USB differential impedance: 90 ohm

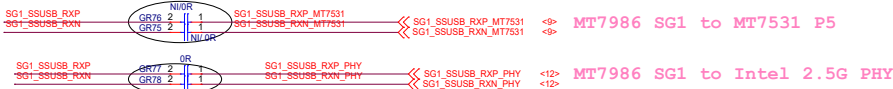
OFF-PAGE CONNECTION



Default BOM SG1 to MT7531A P5

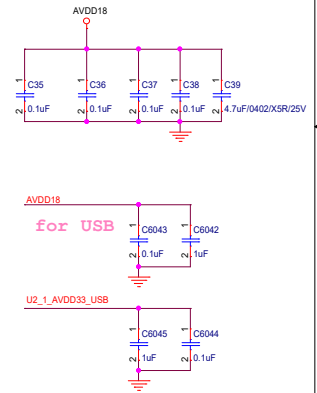
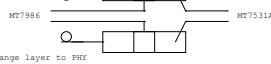


pin 1 Co-pad

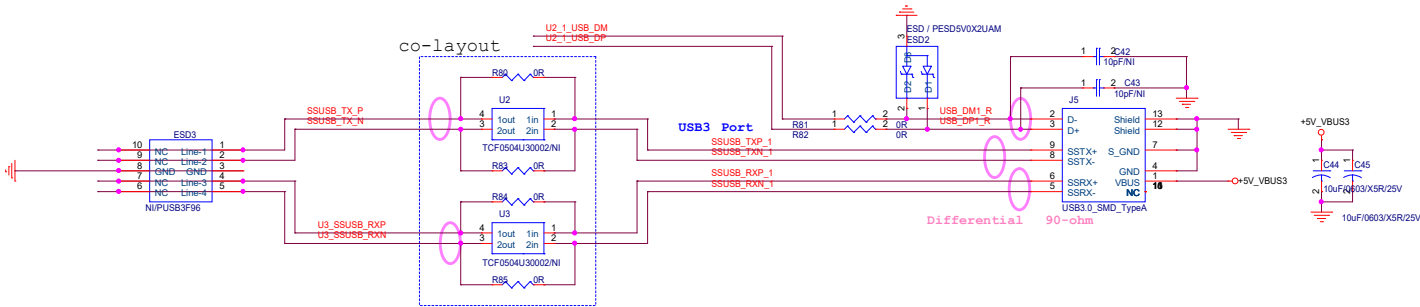


GR72/G73 copad, GR71/GR74 copad
C1075/C5726 copad, C34/C5727 copad

Co-pad



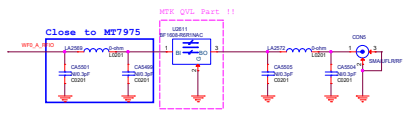
co-layout



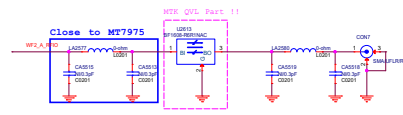
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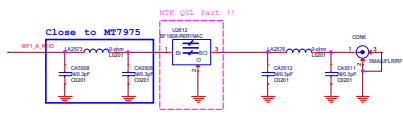
Title: MT7986A_USB_SGMII		Drawn: Steven Kuo	Rev: V10
Size: MT7986A RFB	Document Number: MT7986A RFB	Drawn: Steven Kuo	Rev: V10
Date: Monday, March 28, 2022	Sheet: 6	of: 14	



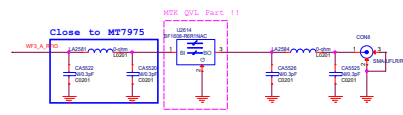
WFO_5G_iPaILNA TX Out Circuit



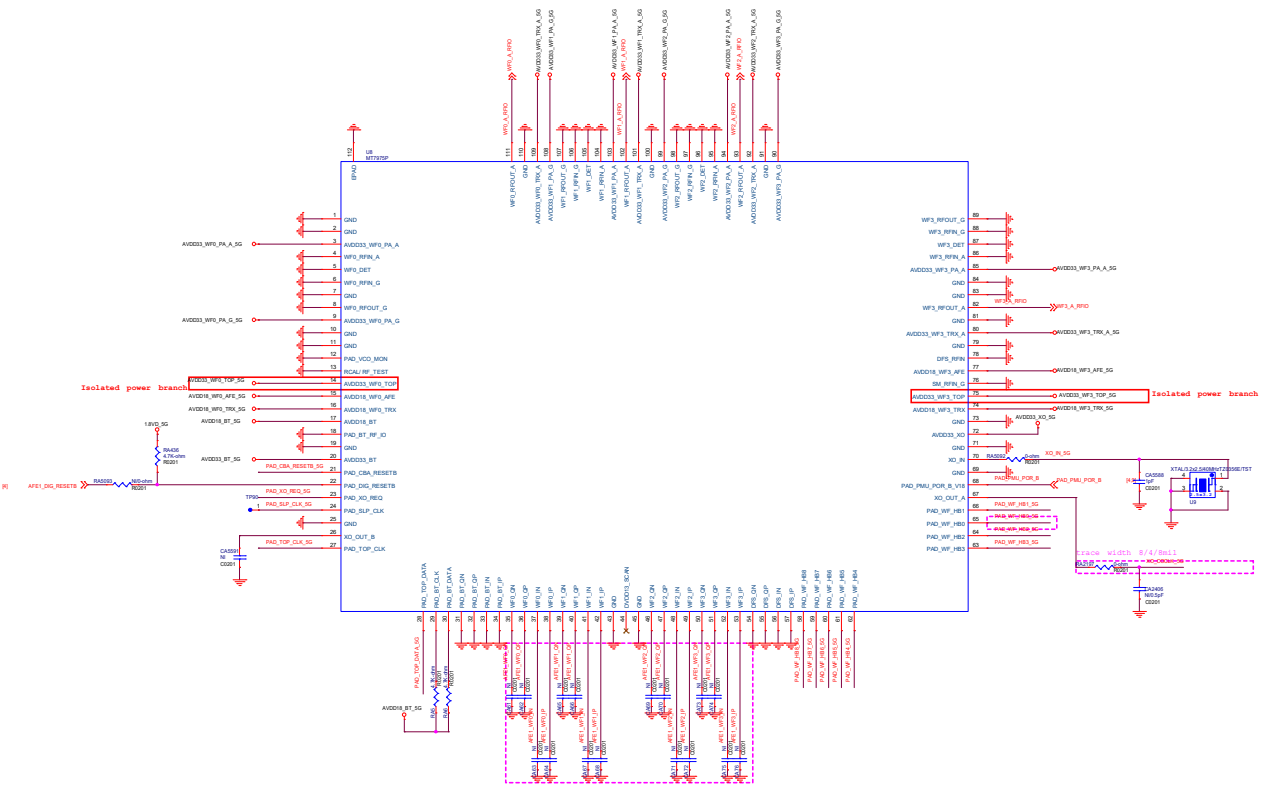
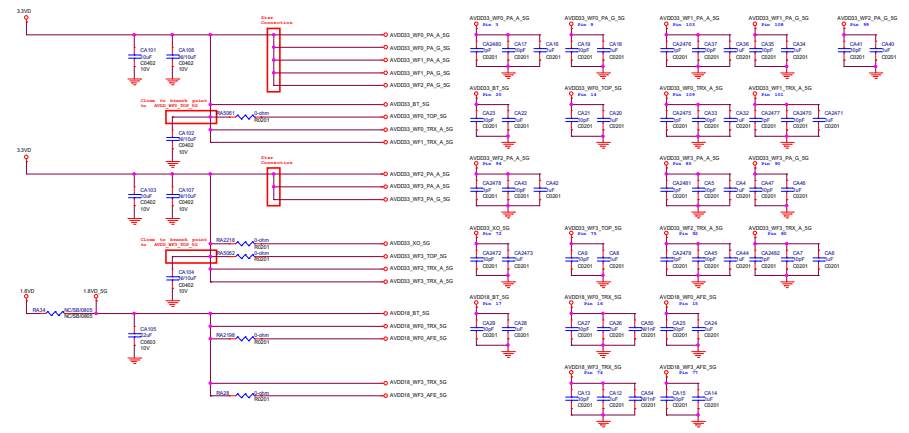
WF2_5G_iPaILNA TX Out Circuit



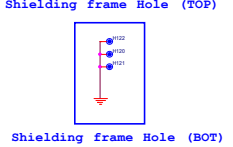
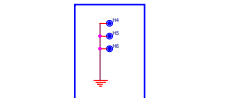
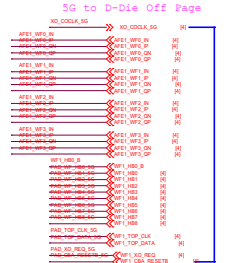
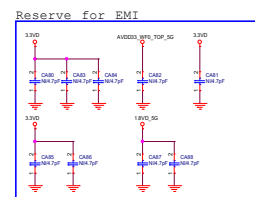
WF1_5G_iPaILNA TX Out Circuit

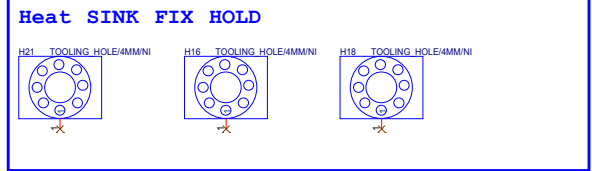
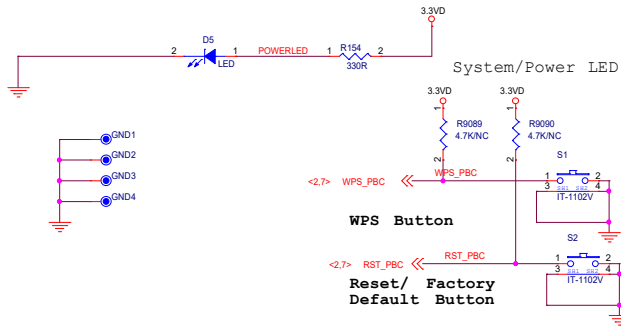


WF3_5G_iPaILNA TX Out Circuit



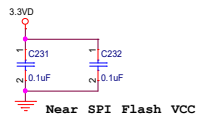
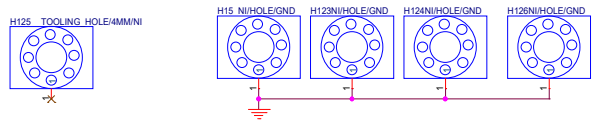
Each IQ Pairs w/ solid GND plane and via (trace width 4/4/0mil)



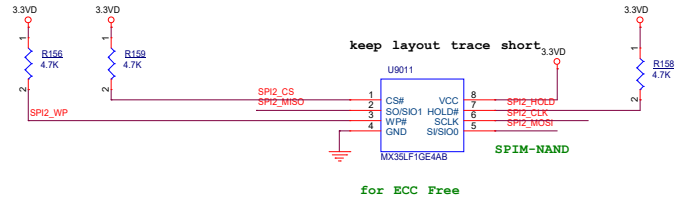


OFF-PAGE CONNECTION

- SPI2_CS <-> SPI2_CS <->
- SPI2_CLK <-> SPI2_CLK <->
- SPI2_MOSI <-> SPI2_MOSI <->
- SPI2_MISO <-> SPI2_MISO <->
- SPI2_HOLD <-> SPI2_HOLD <->
- SPI2_WP <-> SPI2_WP <->
- WPS_PBC <-> WPS_PBC <-2.7>
- RST_PBC <-> RST_PBC <-2.7>
- GPIO_0 <-> GPIO_0 <->
- GPIO_1 <-> GPIO_1 <->
- GPIO_3 <-> GPIO_3 <->
- UART0_TXD <-> UART0_TXD <->
- PWM0 <-> PWM0 <->
- SYS_WATCHDOG <-> SYS_WATCHDOG <->

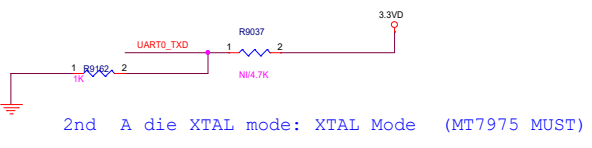
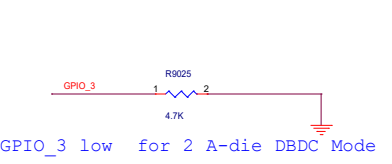
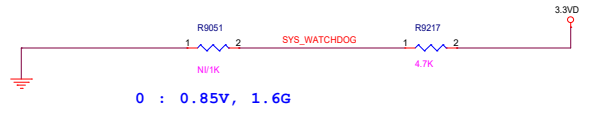
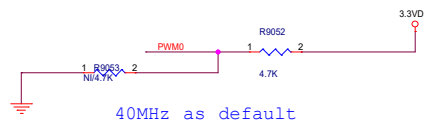
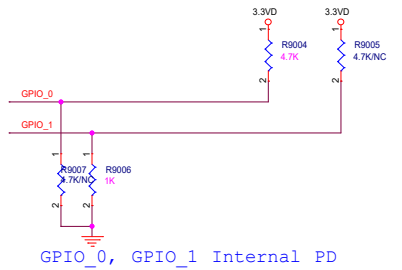


SPI2 to SPIM-NAND Flash



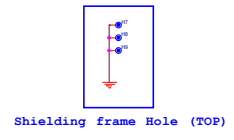
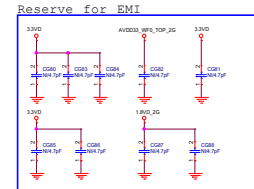
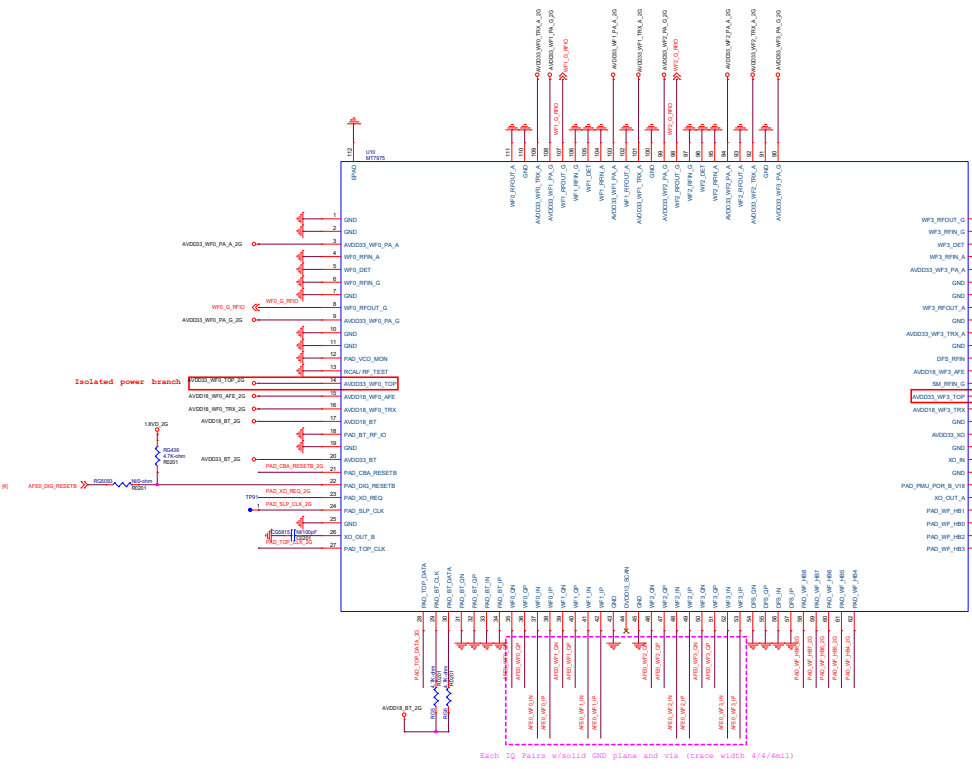
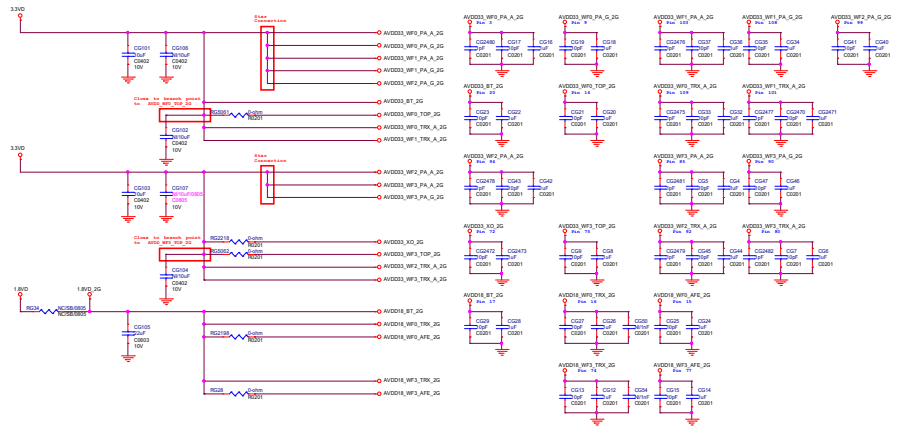
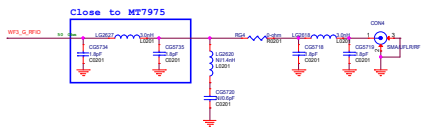
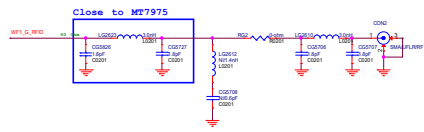
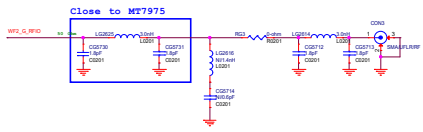
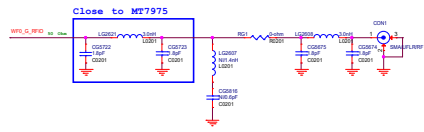
Boot Strapping

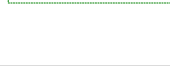
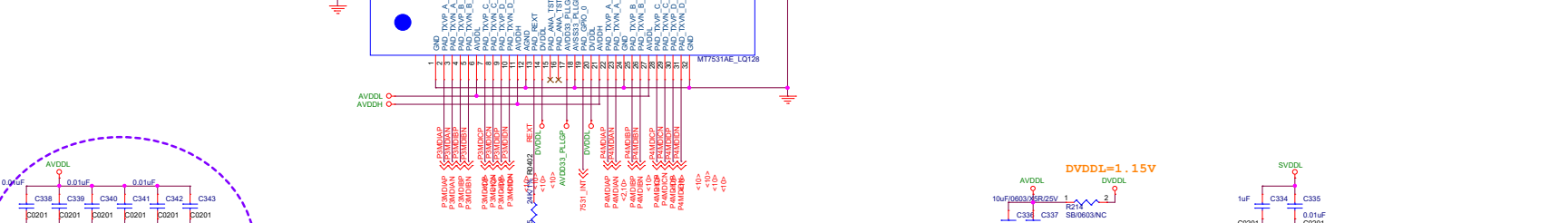
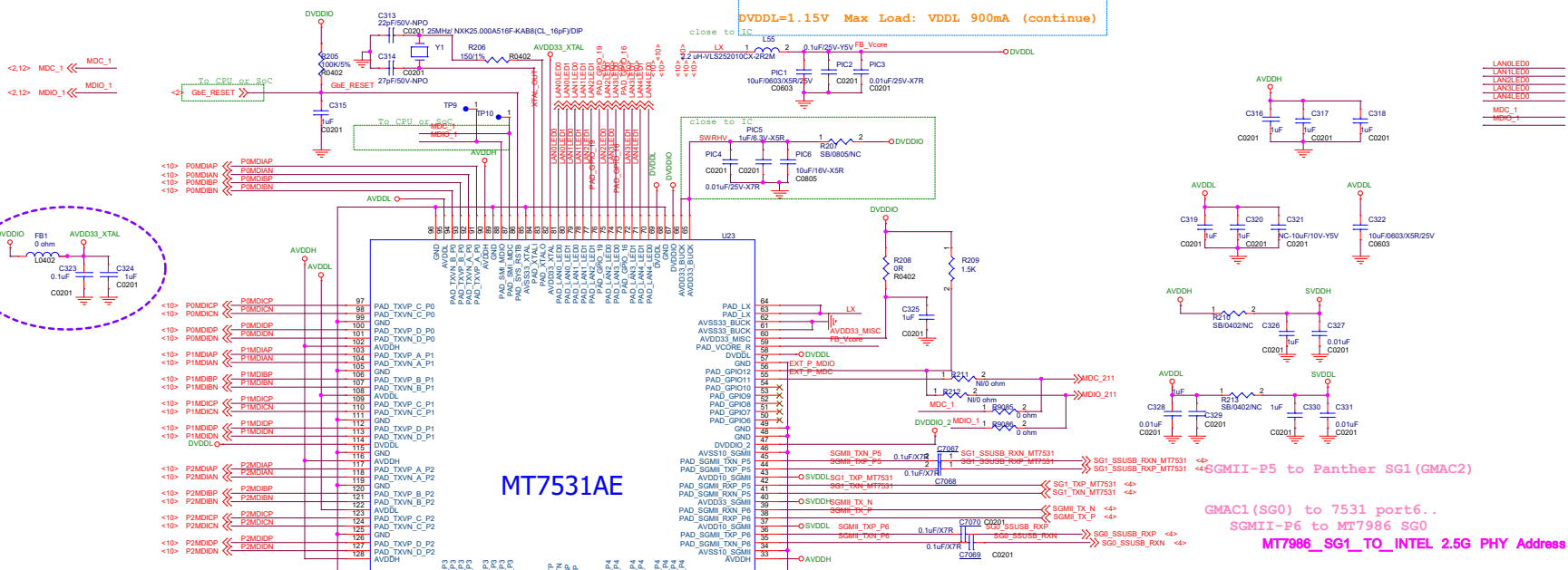
Pin Name	Description	Boot Sequence
{GPIO_1,GPIO_0}	Boot mode	00: SPIM-NOR 01: SPIM-NAND 10: eMMC 11: Reserve
{GPIO_3}	A-Die Mode	0: 2 A-die DBDC 1: 1 A-die DBDC
UART_TX0	Second A Die Xtal mode	0 : XTAL mode <MT7975, MUST> 1 : Buffer mode
PWM0	40MHz Xtal select	1 : 40MHz <default>
SYS_WATCHDOG (MT7986A)	CPU 1.023V/ 0.85V select	0 : 0.85V, 1.6G 1 : 1.023V, 2G

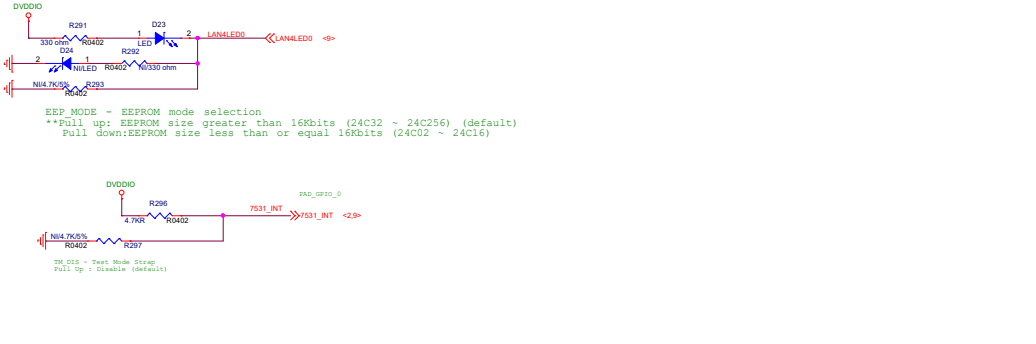
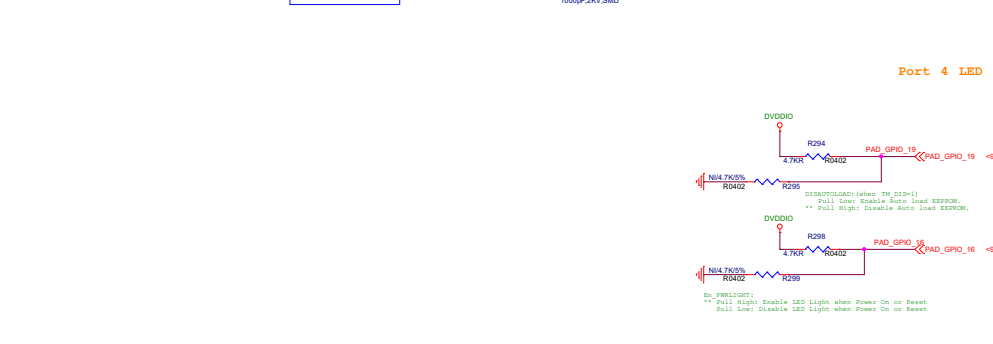
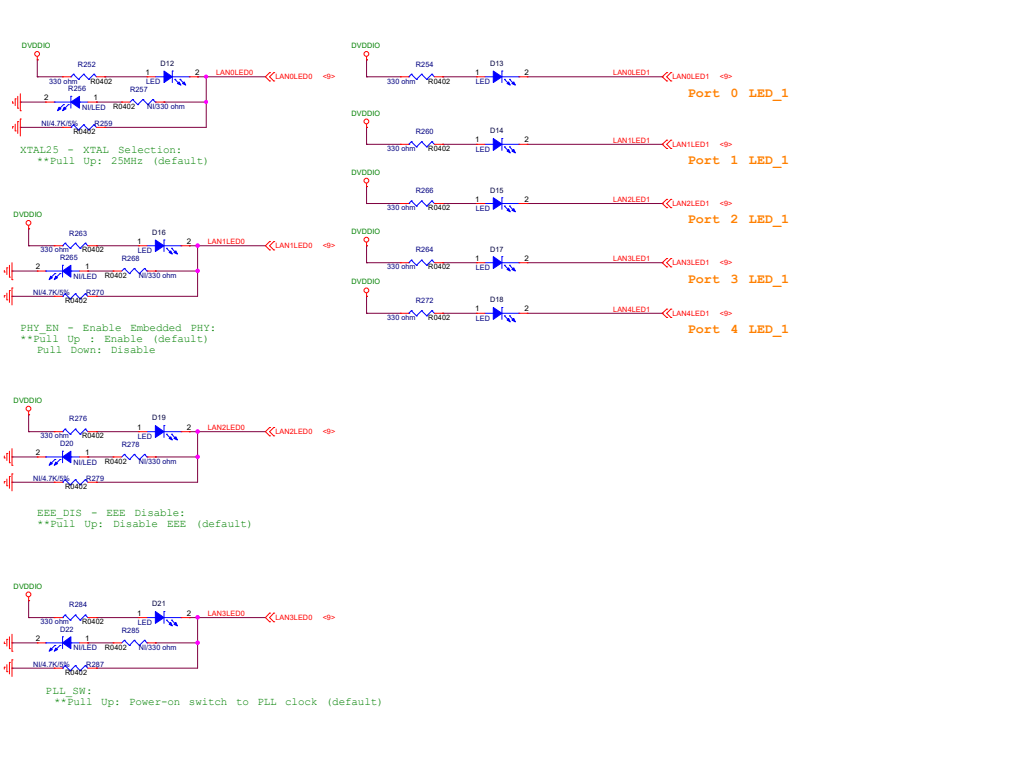
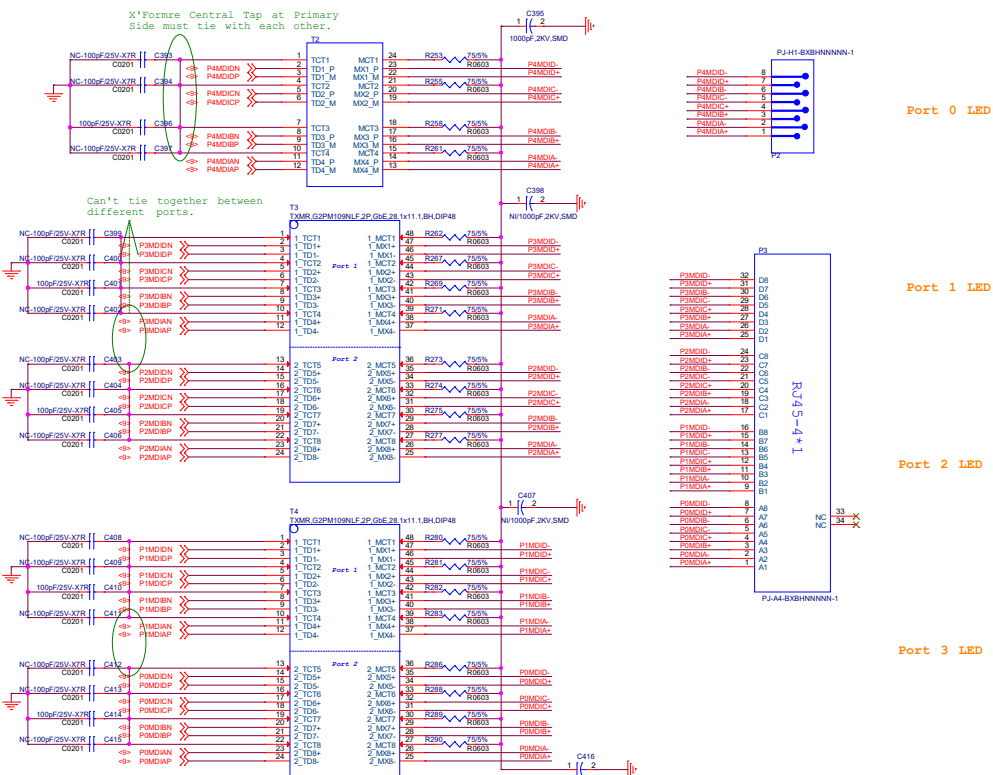


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Flash & LEDs				
Size	Document Number	Drawn	Rev	
C	MT7986A RFB	Slaven Kuo	V10	
Date:	Monday, March 28, 2022	Sheet	9	of 14

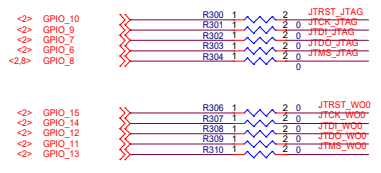






EEP_MODE - EEPROM mode selection
 **Pull up: EEPROM size greater than 16Kbits (24C32 ~ 24C256) (default)
 Pull down: EEPROM size less than or equal 16Kbits (24C02 ~ 24C16)

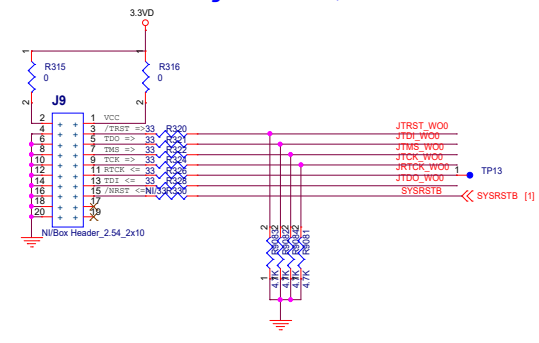
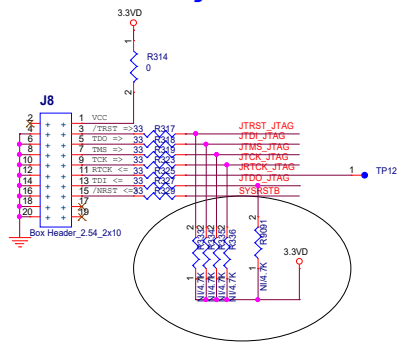
JTAG



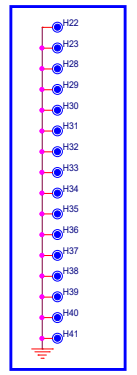
GPIO 6 JTAG_JTRST_N
 GPIO 7 JTAG_JTDI
 GPIO 8 JTAG_JTMS
 GPIO 9 JTAG_JTCLK
 GPIO 10 JTAG_JTRST_N
 GPIO 11 W00_JTAG_JTDO
 GPIO 12 W00_JTAG_JTDI
 GPIO 13 W00_JTAG_JTMS
 GPIO 14 W00_JTAG_JTCLK
 GPIO 15 W00_JTAG_JTRST_N

default- JTAG CA53
sw confiig for W00

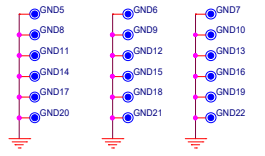
default- JTAG W00
swconfiig for W01



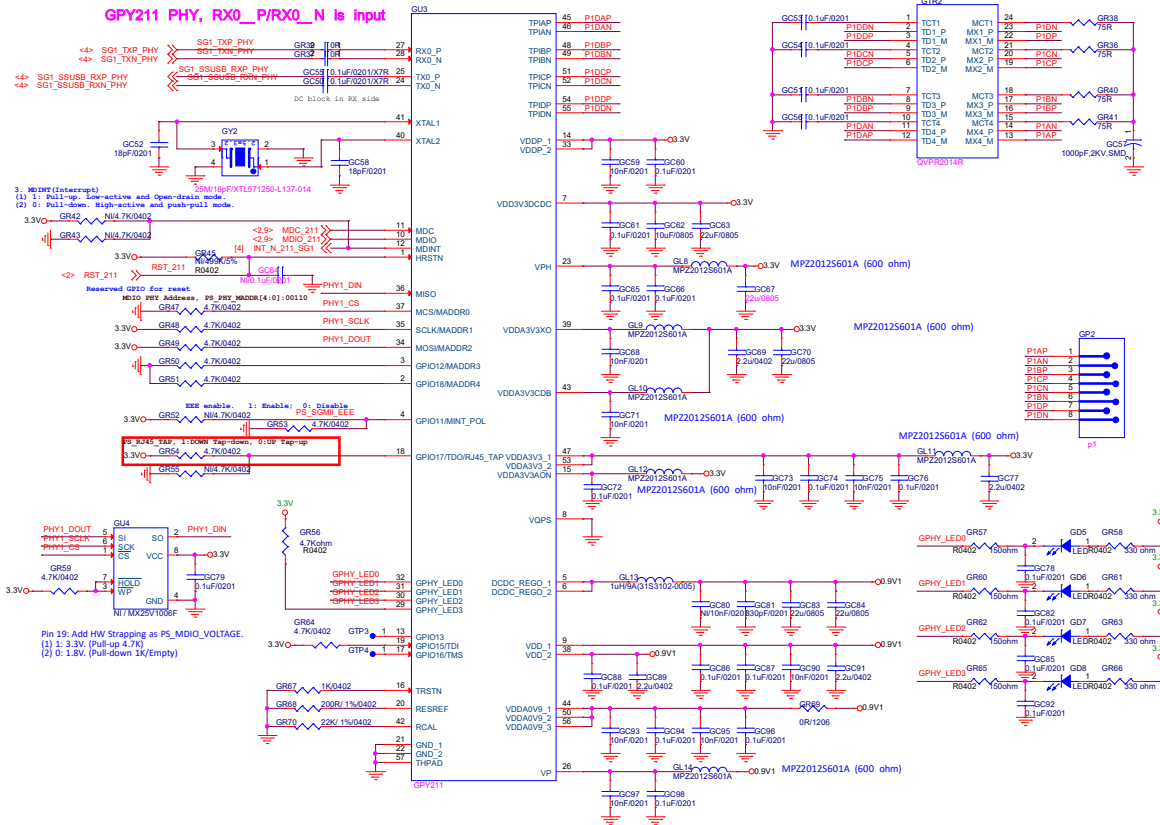
Reserved for debug



Shielding frame Hole



MT7986_SG1_TO_INTEL 2.5G PHY Address 6



GPY211 PHY, RX0_P/RX0_N is Input

